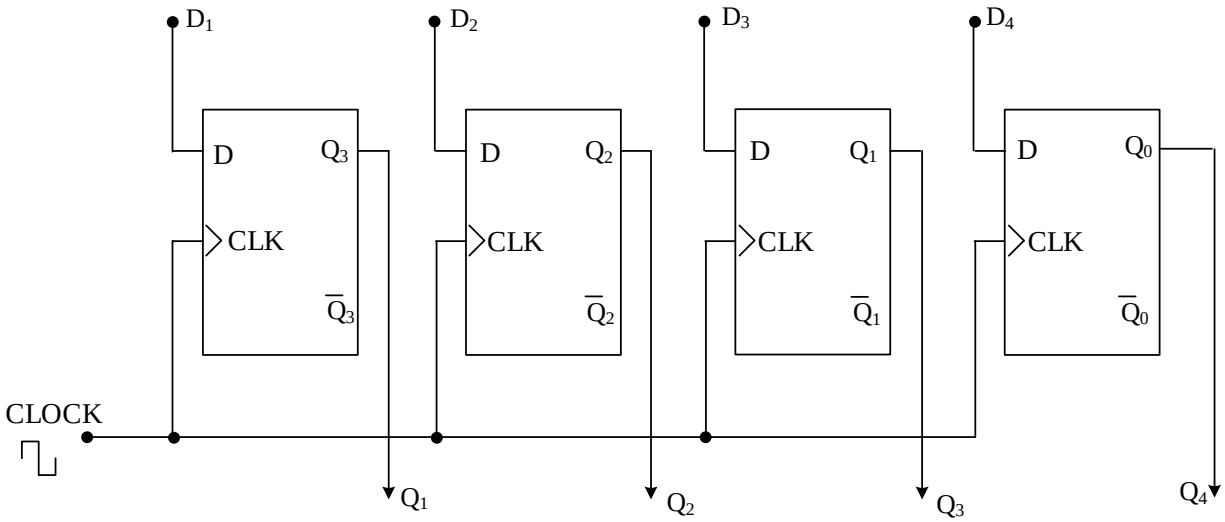
Shift Registers – Sequential Circuits Part III

A register is a group of flip flops suitable for storing binary information. An n- bit register has group of n FFs and is capable of storing binary information containing n bits. Register is mainly used for storing and shifting binary used for storing and shifting binary data entered from external source.

The difference between register and counter is that register has no specific sequence of states except in certain specialized applications.

A simple 4 bit register is shown in figure.



- Common clock pulse
- Information available at 4 inputs (D_1, D_2, D_3, D_4) can be transferred into it
- Four outputs (Q_1, Q_2, Q_3, & Q_4)

Memory register is used to store binary information.

Shift register shifts information either to the right or left.

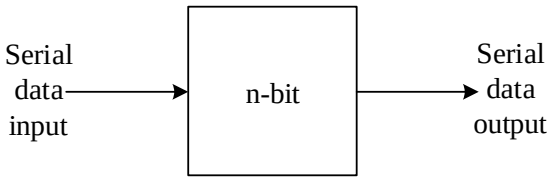
There are two methods of shifting data

(i) Serial shifting – One bit at time
(ii) Parallel shifting – data gets shifted simultaneously, so faster method.

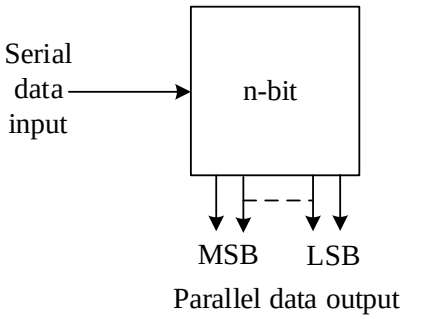
Shift registers are classified into four types:

1. Serial in serial out (SISO)
2. Serial in parallel out (SIPO)
3. Parallel in Serial out (PISO)
4. Parallel in parallel out (PIPO)

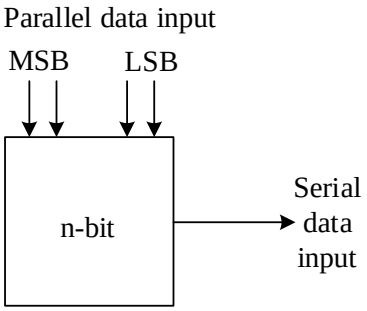
Block diagram representation for four register types is shown in the Fig. using n-bit register.



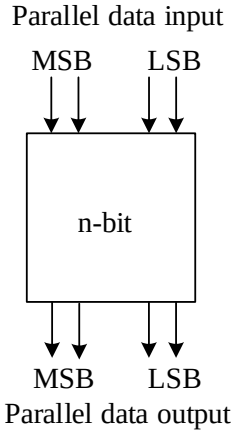
(a) Serial in / Serial output



(b) Serial in / Parallel output



(c) Parallel in / Serial out

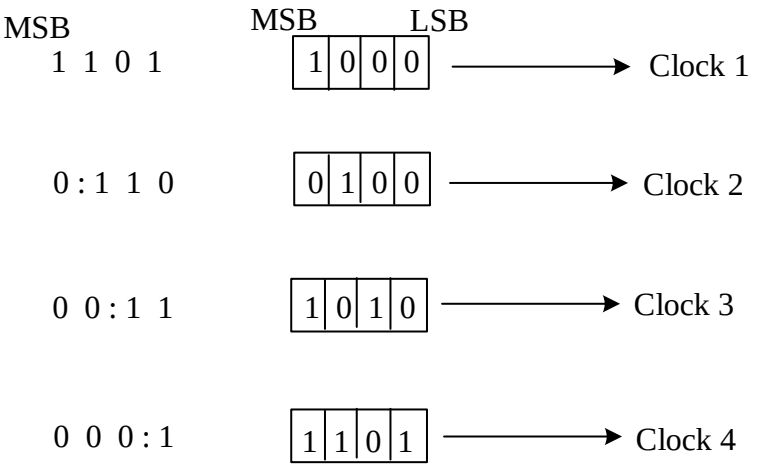


(d) Parallel in / Parallel out

Serial Input/Serial Output Shift Registers:

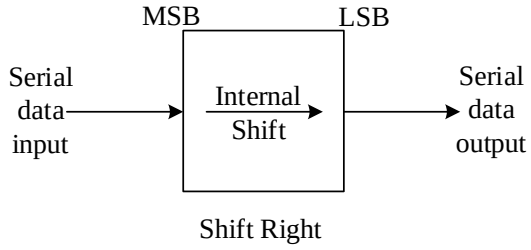
Serial input output registers receive the input data stream one bit at a time on succeeding clock pulses. Data are shifted between register FFs. Each clock pulse causes data stored in one FF to be transferred into next. Serial output is obtained from a single FF at the register end.

Figure illustrates a shift right sequence(4 bit) with internal data shifted from MSB towards LSB. External data are loaded one bit at a time, LSB bit first.

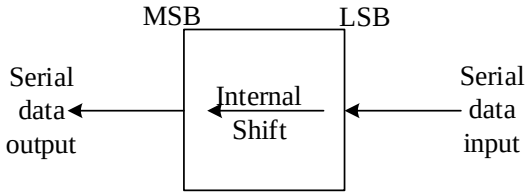


Figures indicate the shift right and left operation.

When starting with MSB and proceeding to LSB the process is shift left



Shift Right



Shift Left

Parallel input / parallel output (PIPO):

To load parallel data each input data bit is presented to respective FF. In synchronous registers an enable input is used in association with clock. In asynchronous parallel load registers operate on level activated enable inputs. PIPO is not a shift register but storage register.

Bi-directional Shift Register: A register that can shift data both to the right and left**.**

Unidirectional register: Shifts data only in one direction.

Universal shift register: If register has shift and parallel load capabilities it is called shift register with parallel load or universal shift register.

Capabilities of a most general shift register:

- Clear control to clear registers.
- CLK input to synchronize all operations.
- Shift right control: Enables shift right operation and serial input output lines.
- Shift left control: Enables shift left operation and serial input output lines.
- Parallel load control to enable parallel transfer.
- n parallel output lines
- A control line.

Shift Register Counters:

Shift register counters use feedback (i.e. last FF output in the register is connected back to the first FF in some way).

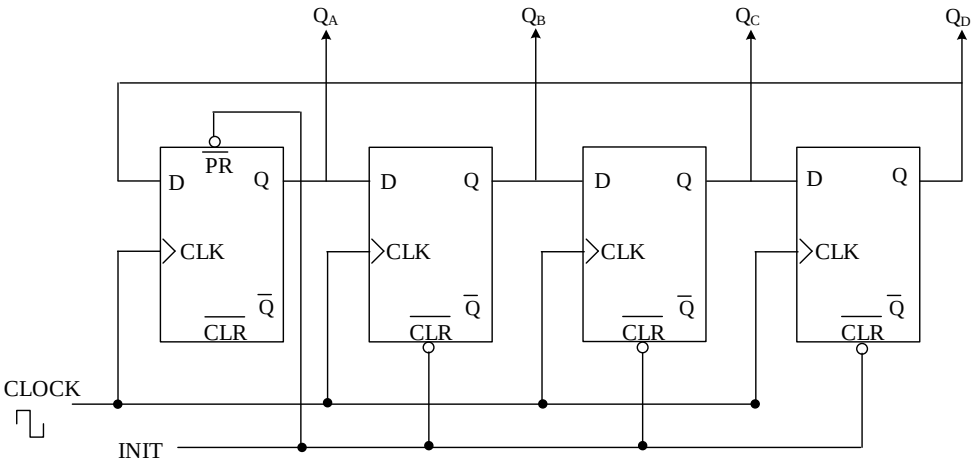
Registers can be arranged to form several types of counters. All shift register counters use feedback. Based on the type of feedback they are classified as ring counter or twisted ring or Johnson counter.

Thus two types of arrangements.

(i) Standard ring or ring counter.
(ii) Twisted ring or Johnson counter or shift counter.

Ring Counter:

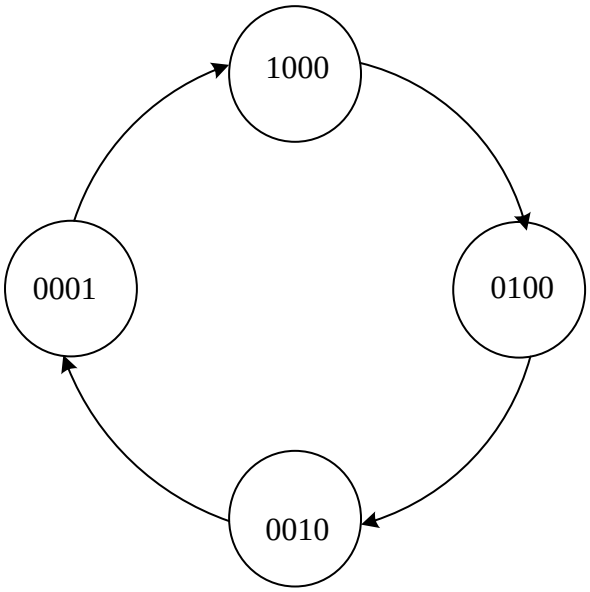
Ring counter is a collection of synchronously clocked FFs usually D FFs. Each FF output is connected to synchronous excitation input of next FF so that data is transferred from left FF to right FF on each clock pulse, much like shift register. The rightmost FF output is fed- back into synchronous input of the left most FF, permitting the content of counter to recirculate.



Separate parallel data inputs permit the parallel loading of all FFs at the same time. Usually the parallel load inputs are asynchronous once data pattern to loaded in the counter it will shift the counter content right on each clock pulse to produce a repeating bit pattern output.

Truth table for 4 bit ring counter

INIT	CLK	Q_A	Q_B	Q_C	Q_D
L	X	1	0	0	0
H	↑	0	1	0	0
H	↑	0	0	1	0
H	↑	0	0	0	1
H	↑	1	0	0	0



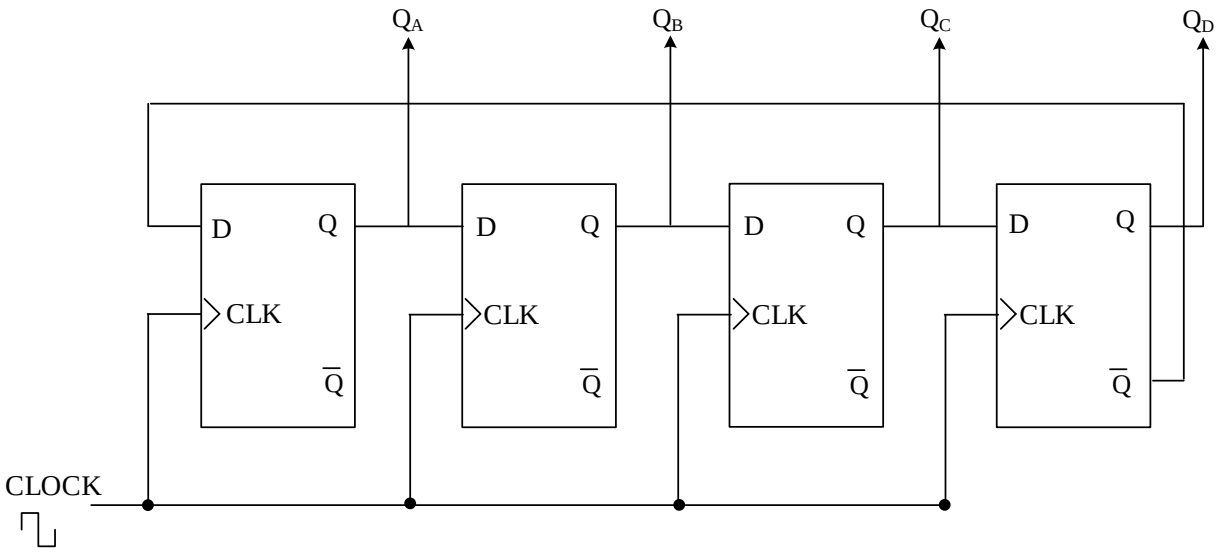
State diagram of 4 bit ring counter

Such bit patterns generated can be useful in generation of timing sequences for control applications.

In this circuit the preset input of first FF and clear of other three FFs are connected together and brought to INIT input. So the first FF is set to 1 and others FFs are cleared to 0.

Johnson Counter or Twisted ring Counter:

The basic ring counter can be modified to produce another type of shift register counter. Johnson counter is constructed exactly like a normal ring counter, except that inverted output of last FF is connected to input of first FF.



Johnson counter operations is easy to analyses. On each +ve clock transit as the level at Q_A shifts into Q_B the level at Q_B shifts into Q_C and Q_C and shifts to Q_D. The inverse of Q_D shifts into Q_A. Truth table is shown in the Figure.

Truth table for 4 bit Johnson counter

CLK	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
↑	1	0	0	0
↑	1	1	0	0
↑	1	1	1	0
↑	1	1	1	1
↑	0	1	1	1
↑	0	0	1	1
↑	0	0	0	1
↑	0	0	0	0

(1) Counter has 8 states 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001 thus it is MOD 8 Johnson counter. If does not count in a normal binary sequence.
(2) Waveform of each FF is square wave.

The MOD number of Johnson counter will always be equal to twice the number off FFs. Thus, it is possible to construct MOD – N counter (where N is even) by connecting N/2 FFs in Johnson counter arrangement.

Comparative Study

Ring Counter	Johnson Counter
1. Synchronous 2. MOD N counter (needs Max no of FFs) 3. Needs no decoding circuitry 4. Output is not square wave. 5. Finds use in generation of timing sequences for control applications.	1. Synchronous 2. MOD 2N counter (needs less FFs than ring binary) 3. More Circuitry (More than ring counter but less than binary counter) 4. Square wave output 5. To produce time delays since the output of each FF is delayed by one clock pulse from previous output