Logic Families

1. VLSI refers to digital ICs having
   a. More than 1000 gates
   b. More than 100 gates
   c. More than 100 but less than 9999
   d. More than 100 but less than 999

2. Typical size of digital IC chip is
   a. $1'' \times 1''$
   b. $2'' \times 2''$
   c. $0.1'' \times 0.1''$
   d. $0.001'' \times 0.001''$

3. IC chip used in digital clock is
   a. SSI
   b. LSI
   c. VLSI
   d. MSI

4. Logic families which are in use now a days are
   a. DTL & EMOS
   b. TTL, ECL, CMOS and RTL
   c. TTL, ECL & CMOS
   d. TTL, ECL, CMOS & DTL

5. ATTL circuit with totempole output has
   a. High output impedance
   b. Low output impedance
   c. Very high output impedance
   d. Any of the above

6. TTL uses
   a. Multi emitter transistor
   b. Multi collector transistor
   c. Multi base transistor
   d. Multi emitter or multi collector transistor

7. Advanced low power schootky is a part of
   a. ECL family
   b. CMOS family
   c. TTL family
   d. None of the above

8. For wired AND connection use
   a. TTL gates with active pull up
   b. TTL gates with open collector
   c. TTL gates without active pull up and with open collector
   d. Any one of the above

9. Time delay of a TTL standard family is above
   a. 180 ns
   b. 50 ns
   c. 18 ns
   d. 3 ns

10. As compared to TTL, ECL has
   a. Lower power dissipation
   b. Lower propagation delay
   c. Higher propagation delay
   d. Higher noise margin

11. As compared to TTL CMOS logic has
   a. Higher speed of operation
   b. Higher power dissipation
   c. Smaller physical size
   d. All the above

12. Which logic family has the highest power dissipation per gate
   a. ECL
   b. TTL
   c. CMOS
   d. PMOS

13. Which is the most commonly used logic family
   a. ECL
   b. TTL
   c. CMOS
   d. PMOS

14. Fill in the banks of the statements below concerning the following logic families:
   Standard TTL (74 XXXLL), Low power TTL (74LXX) Low power Schottky TTL (74L SXX), Schottky TTL (74 SXX), Emitter coupled logic (ECL), CMOS
   a. Among the TTL families, ----------family requires considerably less power than the standard TTL (74 XX) and also has comparable propagation delay.
   b. Only the ---------- family can operate over a wide range of power supply voltages

[GATE 1987: 1 Mark]

15. In the output stage of a standard TTL, we have a diode between the emitter of the pull up transistor and the collector of the pull down transistor. The purpose of this diode is to isolate the output node from the power supply V_{CC}

[GATE 1994: 2 Marks]

16. In standard TTL the 'totem pole stage refers to
    a. The multi-emitter input stage.
    b. The phase splitter
    c. The output buffer
    d. Open collector output stage

[GATE 1997: 1 Mark]

17. The inverter 74 AL S01 has the following specifications:

    The fan out based on the above will be

    a. 10
    b. 20
    c. 60
    d. 100

[GATE 1997: 1 Mark]

18. The noise margin of a TTL gate is about
    a. 0.2 V
    b. 0.4 V
    c. 0.6 V
    d. 0.8 V

[GATE 1998: 1 Mark]

19. A Darlington emitter follower circuit is sometimes used in the output stage of a TTL gate in order to
    a. Increase its to I_{OL}
    b. Reduce its I_{OH}
    c. Increase its speed of operation
    d. Reduce power dissipation

[GATE 1999: 1 Mark]

20. The output of the 74 series GATE of TTL gates is taken from a BJT in
    a. Totem pole and common collector configuration
    b. Either totem pole or open collector configuration
    c. Common base configuration
    d. Common collector configuration

[GATE 2003: 1 Mark]

21. The full forms of the abbreviations TTL and CMOS in reference to logic families are
    a. Triple Transistor Logic and Chip Metal Oxide Semiconductor
    b. Tristate Transistor Logic and Chip Metal Oxide Semiconductor
    c. Transistor Transistor Logic and Complementary Metal Oxide Semiconductor
    d. Tristate Transistor Logic and Complementary Metal Oxide Silicon

[GATE 2009: 1 Mark]

Logic Families

(Answers with brief explanation)

1. (c);
   VLSI refers to very large scale integrated circuits. VLSI is digital system on chip; large memory chips or advanced microprocessors fall in this category.

2. (c);

   Typical chip size ranges from 40 X 40 mils to 300 X 300 mils (where 1 mil = 0.001 inch). So the most appropriate choice is option (c) i.e. $0.1'' \times 0.1''$.

3. (b);
   Digital clock is a typical application of digital counters. DC supply is converted into 60 Hz supply. 60 Hz frequency is divided into seconds, minutes and hours by frequency divider. Output section is digital time display. The processing system consists of gates, Flip flops etc. So the IC chip for digital clock will be LSI.

4. (c),
   Options (a),(b) and (d) involve either DTL or RTL, since they are not in use these days, hence the option is (c) which involves:
   TTL – Most commonly used
   ECL – High speed
   CMOS – Low power consumption

5. (b);
   Note that the top transistor in totem pole configuration works as emitter follower having low output impedance.
   Totem pole output has two transistors one sitting over the other.

6. (a);
   To provide multiple inputs, multiple emitters are used in input transistor. These emitters behave like input diodes in DTL.

7. (c);
   Advanced low power Schottky (ALS) has the advantage of power and speed i.e. minimum power and maximum speed i.e. minimum speed- power product.

8. (b);
   TTL in open collector configuration provides wired logic while totem pole does not provide.

9. (c);
   The value of time delay as quoted in manuals is around 10ns. So option (c) of 18 n sec. seems to be the best choice.

10. (b);
    ECL has lowest propagation delay (highest speed). Although its power consumption is highest.

11. (c);
    CMOS has smaller physical size as compared to TTL (N-MOS and P-MOS ICs have greater packing density than C-MOS)

12. (a);
    ECL has the highest power dissipation.

13.(b);

Most commonly used logic family. Earlier it was used for SSIs & MSIs. Now it is competing with MOS with its sub families like 74S, 74LS, 74ALS, etc.

14.(a);

Out of the given families 74 LS XX (Low power Schottky) is the best choice. Since it has considerable less power dissipation, say about 2mW as compared to standard TTL. And also it has comparable propagation delay typical 9.5 ns.

(b);

CMOS family provides the widest range of supply voltage i.e. upto 18V

15.The purpose of diode in the output of TTL circuit is to keep pull up (top) transistor in off state as long as pull down (bottom) transistor is in ON state The voltage drop at diode keeps base to emitter junction of pull up transistor reverse biased.

16.c;

Totem pole is the output stage of TTL gate. The name totem pole is due to apparent stacking of one transistor on top of another, in a fashion resembling the totem poles of northwest Indian tribes. Here only one of the transistor is on at a time. So it is the output buffer stage.

17.(b);

$$(FO)_H = (Fan\ out)_H = \frac{I_{OH(\max)}}{I_{IH(max)}} = \frac{0.4X10^{-3}}{20X10^{-6}} = \frac{400}{20} = 20$$

$$(FO)_L = (Fan\ out)_L = \frac{I_{OL(max)}}{I_{IL(max)}} = \frac{8 \times 10^{-3}}{0.1 \times 10^{-3}} = 80$$

$Fan\ out = min\ of[(FO)_H, (FO)_L]$

Min of [20, 80]

Fan Out = 20

18.(b);

For TTL

Noise margin $(H) = V_{NH} = (V_{OH} - V_{IH}) = 2.4 - 2.0 = 0.4$

Noise margin $(L) = V_{NL} = (V_{IL} - V_{OL}) = 0.8 - 0.4 = 0.4$

So N.M = 0.4 V

19.(c);

Note that 74S circuits use Darlington pair in the output stage to provide shorter rise time when switching from ON to OFF (since its output impedance is very low).

20.(a);

Totem pole output provides

(i) Fast switching times

(ii) Low power dissipation

But also provides large current spikes during switching from low to high.

21.(c)

Transistor Transistor Logic (TTL): It is bipolar logic family that has evolved from DTL.

Complementary Metal Oxide Semiconductor CMOS: It consists of circuit consisting of both N and P channel field effect transistors.