Digital Integrated Circuits – Logic Families (Pt.I)

Integrated circuits classified as

(i) Linear (ii) Digital

Digital ICs classified as per level of integration.

These are like SSI, MSI, LSI, VLSI, ULSI and GSI as per the number of Gates.

SSI (<12), MSI (12 to 99), LSI (100 to 9999), VLSI (10,000 to 99,999), ULSI (100,000 to 999,999) & GSI (1 Million or more)

SSI - Basic gates & FFs

MSI - More complex like adders, comparators

LSI - Small digital systems like digital clocks calculator

VLSI - Digital system on chip like large memory chips

ULSI & GSI - Complex function – several boards of ICs

Logic Families

(i) Bipolar
- Saturated (RTL, DCTL, DTL, TTL, I^2L)
- Non Saturated (Schottky TTL & ECL)

(ii) MOS Families (P MOS, N MOS, C MOS)

Digital IC Characteristics

(1) Current and voltage parameters

They are: I_{IH}, I_{IL}, I_{OH}, I_{OL} And V_{IH}, V_{IL}, V_{OL} & V_{OH}

V_{IH} → Minimum voltage level required for logic 1 at input .For TTL, it is 2.0V

(2) Propagation delay (t_{pd}) ; Delay time in going from low to high logic or high to low logic (t_{pLH} & t_{pHL})

$t_{pd} = (t_{pLH} + t_{pHL}) / 2$

In BJT $t_{pLH} > t_{pHL}$ (Due to reverse recovery)

In FET $t_{pLH} < t_{pHL}$ (Due to large capacitance)

Typical 15 ns (for TTL)

(3) Power dissipation

It is a measure of power consumed by logic gate when fully driven. Avg. power dissipated is product of DC supply voltage and mean current.

For TTL standard it is 10 mW

(4) **Fan in & Fan out**

Fan in – No. of inputs connected to gate without degradation

Fan out – Max number of similar gates that gate can drive

Typical, fan out 10 for TTL.

$(\text{Fan out})_H = I_{OH} / I_{IH}$ And $(\text{Fan out})_L = I_{OL} / I_{IL}$

Overall Fan out is lowest of the two.

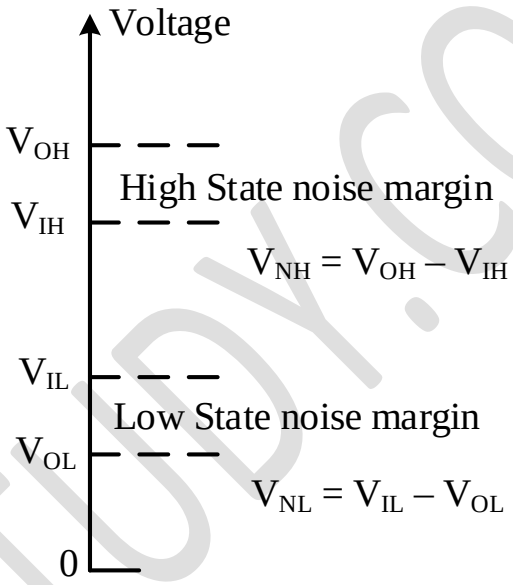
(5) Noise immunity or Noise Margin : It is the ability of the circuit to tolerate noise without causing spurious changes in the output

For TTL

$V_{NH} = 2.4 – 2.0 = 0.4$

$V_{NL} = 0.8 – 0.4 = 0.4$

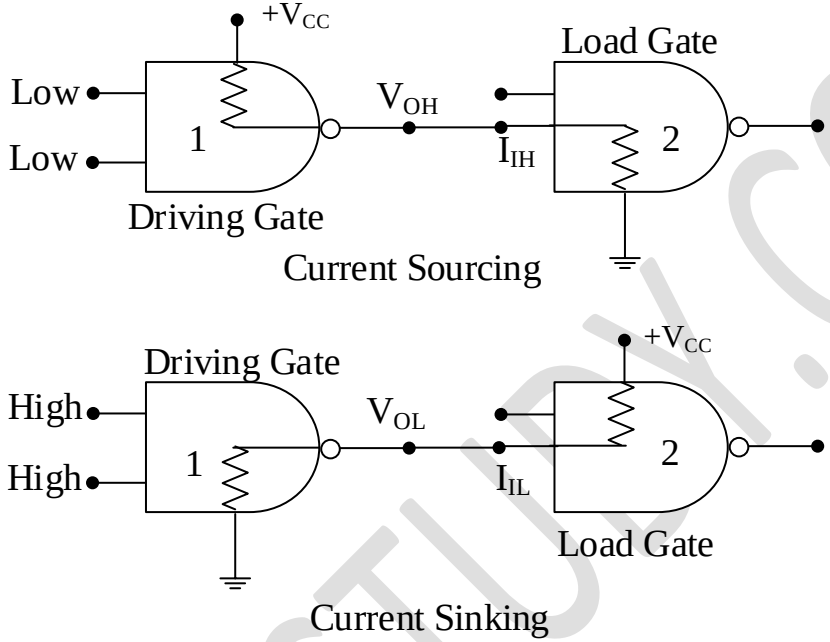
NM For TTL 0.4 V



(6) Current Sourcing & Sinking

Current sourcing: Output supplies (sources) current to load circuit. For TTL it is 40 µA.

Current Sinking: Output receives (sinks) current from the input of the load gate. For TTL it is 1.6 mA



(7) Speed Power Products or Figure of Merit(FOM) :

Speed power product $t_{pd} \times P_{Davg}$

$10\ ns\ \times 5\ mw$

$$50\ pico - Joules\ (PJ)$$

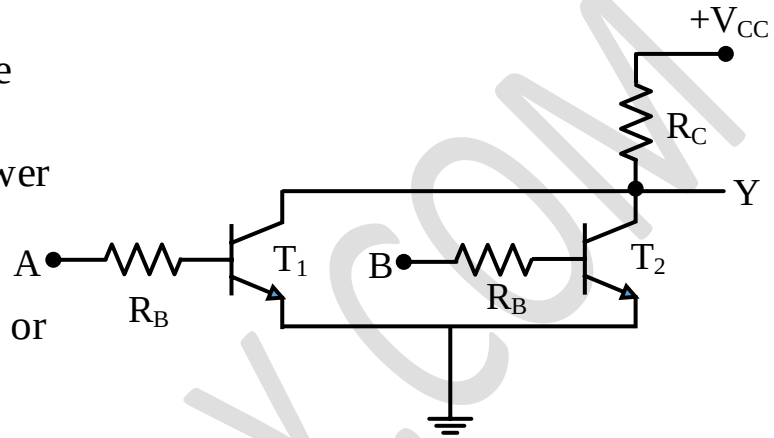
When delay in ns & P_{avg} in mw, speed power
Product in pico – Joules
Low value desirable.
For TTL (Std.) – 100 pico - Joules

Bipolar Logic Families

Bipolar ICs use resistors, BJT, and diodes. They are either saturated logic or non- saturated.

(1) Resistor Transistor Logic (RTL)

- Earliest, in use before development of ICs
- Low speed, High power dissipation and low Fan out
- Can be used in wired or connection



(2) Direct coupled Transistor Logic (DCTL)

- Base resistors R_B not used
- Logic levels are $V_{BE(sat)}$ = 0.8 V & $V_{CE(sat)}$ = 0.2 V
- Simpler than RTL
- Poor noise margin
- Problem of current hogging

(3) Diode transistor Logic (DTL)

- First cct.config.to be designed as IC. Uses diode AND and BJT inverter.

- It has limitation of no low and constant output impedance in both the states.

(4) Transistor Transistor Logic (TTL)

Problem of DTL eliminated by totem pole output.

Q_1 – Multiple emitter transistor

Q_2 – Phase splitter

Q_3 & Q_4 – Totem pole output.

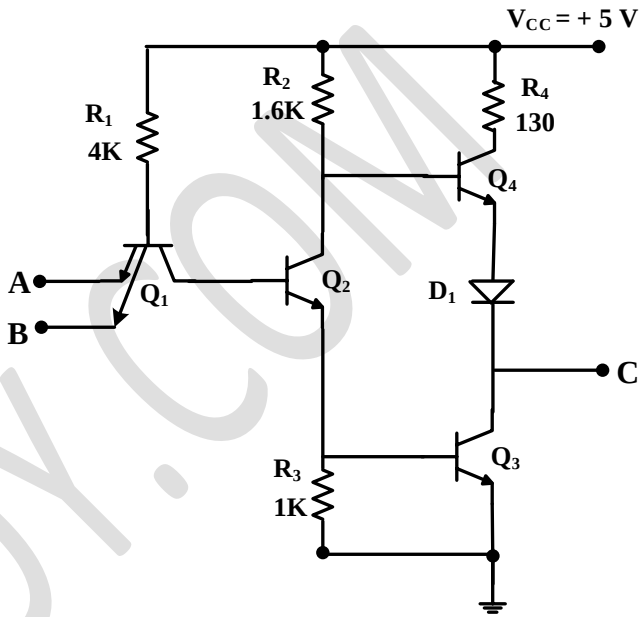
Diode D ensures that Q_4 cutoff when output low

A = B = 0 E – B Jns forward biased

Q_1 saturates

Q_2 base voltage '0' so cutoff

Q_3 in cutoff & Q_4 acts like Emitter follower.



Output is high

A = B = 1: E – B Jun. Rev. Biased & C-B Jun. For. Biased.

Q_1 is in rev. active mode, current into base of Q_2, so saturates.

Voltage at collector of Q_2= 0.8V = 0.7 + 0.1 V, so Q_4 not turned ON , Q_3 saturates **low output**

Totem pole output: Fast Switching speed and low power dissipation.

Large spike while switching from low to high.

Open collector output: Wired AND & OR operation.

Tristate output: Incorporates benefit of totem pole and open collector.

TTL sub families are in common use.

Schottky TTL:

- The main purpose is to increase speed.
- Four sub families that use Schottky diodes and transistors (74S, 74LS, 74ALS and 74AS).
- Schottky transistor use Schottky clamp diode across collector base junction of BJT to prevent its saturation.
- Schottky carrier diodes are also called hot carrier diodes.

TTL sub families speed- power comparison

Minimizing Power				Minimizing delay time			
Family	Propagation Delay (ns)	Power Dissipation (mW)	Speed/Power Product (pJ)	Family	Propagation Delay (ns)	Power Dissipation (mW)	SPD/PWR Product (pJ)
TTL	10	10	100	TTL	10	10	100
L TTL	33	1	33	H TTL	6	22	132
LS TTL	9	2	18	S TTL	3	19	67
ALS	4	1.2	4.8	AS	1.7	8	13.6

- Two approaches (i)Minimizing power (ii)minimizing delay time
- LTTL, LSTTL, ALS all have letter L for low power. ALS series has the best characteristics.
- HTTL, STTL, AS are high speed.**AS is the best.**

- Separate tables help us to visualize.

Comparison of TTL Subfamilies

TTL Sub Families	**Introduction**	**Features**	**Limitations**
TTL Std. (74)	Uses transistors in totem pole output configuration.	Most commonly used as SSI for lab expt.	Low speed & high power dissip.(10ns,10mw)
Low Power TTL (74L)	Increased resistor values.	Reduced power dissipation (1mW) Batt. operated ccts.	High prop. delay Typically 33ns.
High speed TTL (74 H)	Smaller resistor values Emitter follower with Darling. pair	High speed Approx. Prop. Delay 6 ns	More power dissipation Approx. 22 mW

Schottky TTL (74S)	Unsaturated Schottky diode Darlington active pull up	Improved switching speed Approx. 3 ns	Average power dissipation approx.. 20 mW
Low Power TTL (74LS)	Increasing internal resistance Uses Schott. diode	Low power = 2 mW Speed = 9.5 ns	
Advanced Schottky TTL (74 AS)	Smaller device geometries reducing capacitance	Fastest logic family prop. delay 1.7 ns Suitable for high frequencies.	Moderate power dissipation about 8mW
Adv. Low power Schottky TTL(74ALS)	Uses complex circuit	Best for battery op. cct. Lowest speed power product 4.8pJ	

Integrated Injection Logic (I^2 L):

- Also called merged transistor logic

- Uses both npn and pnp transistors
- Reduces number of metal interconnections
- High speed and less power dissipation .Best Figure of merit.
- Finds use in large computers

Emitter Coupled Logic (ECL)

- Current mode logic and non- saturated
- Fastest switching speed (Prop. Delay approx.1 ns)
- High dissipation and takes large chip area
- Circuit consists of differential amplifier and emitter follower

Comparison of Bipolar Logic Families

Name	**Introduction**	**Features**	**Limitations**
Resistor Transistor Logic (RTL)	In common use before development of ICs	First logic family	Low speed High power dissipation &Low Fan out

Direct coupled Transistor logic (DCTL)	Direct Coupled Base resistor of RTL omitted	Simpler than RTL	Small logic swing Power margin
Diode Transistor Logic (DTL)	Uses diode & transistor	First circuit. Configuration Designed into IC.	No low and constant output impedance in both states
Transistor Transistor Logic (TTL)	Uses all transistors Totem pole output	Fast switching time Low power dissipation	Large current spike when switching from low to high
Integrated Injection Logic (I^2L)	Technology of merged transistor logic (MTL) Both p np & n p n transistors are used. Low metal interconnections.	High component density Less power dissipation Used in large computers.	Low speed Poor noise immunity

Emitter Coupled Logic(ECL)	Non saturated logic Complementary output Logic levels -0.8 logic 1 -1.7 logic 0	Fastest logic devices used in very high frequency applications No noise spikes	High power dissipation. Inconvenient voltage levels. Low noise margin