P N Junction Theory and diodes (Part II) – GATE Problems

1. The diffusion capacitance of a P – N junction
   (a) Decreases with increasing current and increasing temperature
   (b) Decreases with decreasing current and increasing temperature
   (c) Increases with increasing current and increasing temperature
   (d) Does not depend on current and temperature

[GATE 19987: 2 Marks]

Soln. **Diffusion capacitance exists when the junction is forward biased. The value of Diffusion capacitance (C_D) is usually much greater than transition Capacitance (C_T). Diffusion capacitance is important for minority change carriers.**

It is given by the following relation

$$C_D = \frac{\tau I}{\eta V_T}$$

Where,

τ **– Mean life time of carriers**

I – forward current

η **– A constant**

= 1 for Ge

= 2 for Si

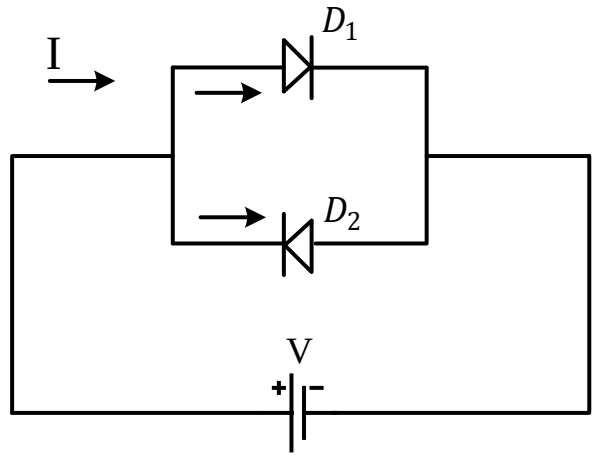
V_T – volt equivalent of temperature

$$\left(V_T = \frac{T}{11,600}\right)$$

If the current decreases the value of C_D also decreases. Also with temperature the value of C_D decreases.

Option (b)

2. In the circuit shown below the current voltage relationship, when D_1 and D_2 are identical is given by (Assume Ge diodes)



(a) $V = \frac{KT}{q}\sinh\left(\frac{I}{2}\right)$

(b) $V = \frac{KT}{q}\ln\left(\frac{I}{I_0}\right)$

(c) $V = \frac{KT}{q}\sinh^{-1}\left(\frac{I}{2}\right)$

(d) $V = \frac{KT}{q}(e^{-1} - 1)$

[GATE 1988: 2 Marks]

Soln. **In the given circuit diode D_1 is forward biased while D_2 is reverse biased. Thus the current through D_1 is forward current I_{D_1} and current through D_2 is *reverse current* (I_{D_2}). As per circuit the total current is given by**

$$I = I_{D_1} + I_{D_2}$$

Diode current is given by

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

Where,

V – Diode voltage

T – Temp ^{o} K

η = 1 for Ge diode

= 2 for Si diode for current below knee voltage

η = 1 for both Ge & Si for large currents.

Current I is given by

$$I = I_0\left(e^{V/\eta V_T} - 1\right) + I_0$$

$$= I_0\, e^{V/\eta V_T}$$

$$or \quad \frac{I}{I_0} = e^{V/\eta V_T}$$

$$or \quad V = \eta\, V_T \ln\left(\frac{I}{I_0}\right)$$

Assume $\eta = 1$

$$V = \frac{kT}{q} \ln\left(\frac{I}{I_0}\right)$$

Option (b)

3. The switching speed of p^+n junction (having a heavily doped P region) depends primarily on
   (a) The mobility of minority carriers in the P^+ region
   (b) The lifetime of minority carriers in the P^+ region
   (c) The mobility of majority carriers in the N region
   (d) The lifetime of majority carriers in the N region

[GATE 1989: 2 Marks]

Soln. The P^+N diode has heavily doped P- region. Under forward bias electrons are injected from N region to P region and holes are injected form P region into the N region. These injected carries become minority carriers in the other region and recombine with the majority carriers there and decay exponentially with distance.

The switching speed of P^+N (heavily doped P – region) junction depends on the life time (τ) of the majority carriers (i.e. electrons) in the N – region which is lightly doped region.

Thus

Option (d)

4. In a Zener diode
   (a) Only the P – region is heavily doped.
   (b) Only the N – region is heavily doped.
   (c) Both P and N – region are heavily doped.
   (d) Both P and N – region are lightly doped.

[GATE 1989: 2 Marks]

Soln. Zener breakdown takes place in a very thin junction. When both sides of the junction are very heavily doped and thus the depletion layer is narrow. In Zener breakdown mechanism electric field becomes very high in depletion layer with only small reverse bias voltage.

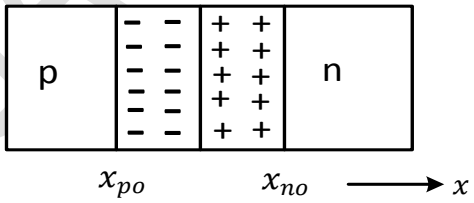
In the process some electrons jump across the barrier from valence band in p material to some unfilled conduction band in n – material. This is known as Zener breakdown.

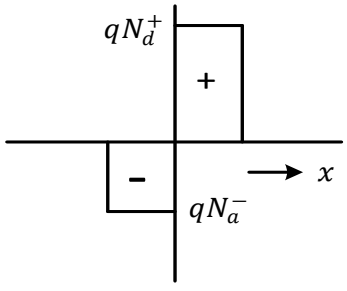
Option (c)

5. In a uniformly doped abrupt P – N junction the doping level of the n – side is four times the doping level of the p – side the ratio of the depletion layer width of n – side verses p – side is
   (a) 0.25 (c) 1.0
   (b) 0.5 (d) 2.0

[GATE 1990: 2 Marks]

Soln. In the transition region of P – N junction electrons and holes are in transit from one side of the junction to the other side. Some electrons diffuse from n top and some are swept by electric filed from p to n.





Space charge neutrality of the semiconductor requires total negative space charge per unit area in the p side must be equal to total positive space charge per unit area in the n side.

$$N_A^- \, . \, x_{po} \;\; = \;\; N_D^+ \, . \, x_{no}$$

The +ve and –ve signs on N_A and N_D indicate the type of space charge

$$or, \qquad \frac{x_{no}}{x_{po}} = \frac{N_A^-}{N_D^+} = \frac{N_A^-}{4N_A^-} = \frac{1}{4} = 0.25$$

Option (a)

6. The small signal capacitance of an abrupt P^+ - N junction is 1 nF at zero bias. If the built–in voltage is 1 volt, the capacitance at a reverse bias voltage of 99 volts is
   (a) 10 (c) 0.01
   (b) 0.1 (d) 100

[GATE 1991: 2 Marks]

Soln. Given,

Capacitance at zero bias 1nF. Find capacitance at reverse bias of 99V.

Reverse bias capacitance is called depletion capacitance or junction capacitance and is given by

$$C_j = \frac{K}{(V_B - V_R)^n}$$

Where

V_B – Barrier voltage

V_R – Applied voltage bias

$n = \frac{1}{2}$ **for step junction**

$\frac{1}{3}$ **for linearly graded junction**

Since junction is abrupt

$$C_{j0}(C_j \; at \; 0V) = \frac{K}{(1+0)^{1/2}} = K$$

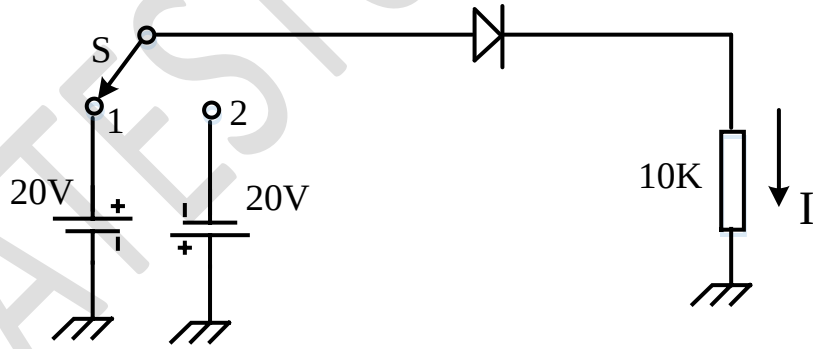
$$C_{j99}(C_j \; at \; 99V \; Rev.bias) = \frac{K}{(1+99)^{1/2}} = \frac{K}{10}$$

$$\frac{C_{j0}}{C_{j99}} = \frac{K}{K/10} = 10$$

$$or, \quad C_{j99} = \frac{C_{j0}}{10} = \frac{1nF}{10} = 0.1nF$$

Option (b)

7. Referring to the below figure the switch S is in position 1 initially and steady state condition exist from time $t = 0 \; to \; t = t_0$. At $t = t_0$, the switch is suddenly thrown into position 2. The current I through the 10K resistor as a function of time t, from t = 0 is _____
(Give the sketch showing the magnitudes of the current at $t = 0, t = t_0 \; and \; t = \infty$).



Soln. In the given problem when the switch is in position 1 diode is forward biased from $t = 0 \;\; to \;\; t = t_0$.

Then switch is suddenly thrown to position 2 (Reverse biased)

When diode is instantaneously switched from conduction state it needs some time to return to non – conduction state, so diode behaves as short circuit for the little time even in reverse direction. This is due to accumulation of stored excess minority charges when diode was forward biased.

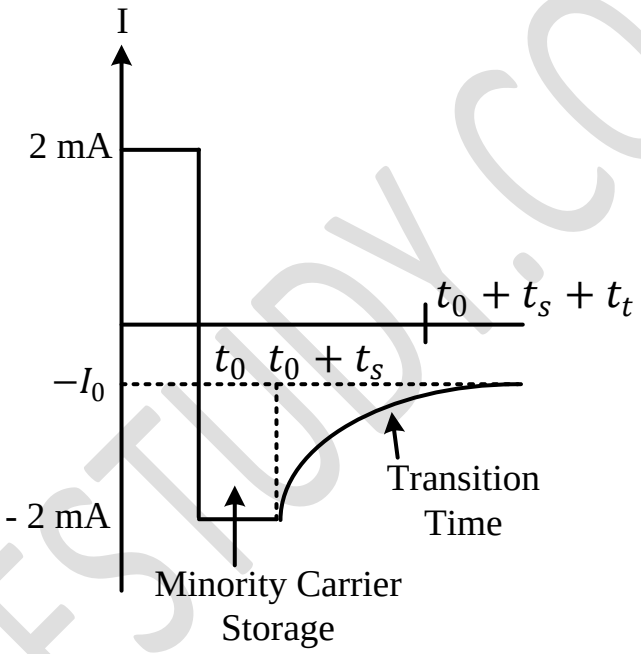
The time required to return back to state of non – conduction is reverse recovery time which is

Storage time (ts) + transition time (t_t)

$$i_F = \frac{V}{R} = \frac{20}{10K\Omega} = 2mA \quad 0 < t < t_0, \; V = 20V$$

$$For \quad t_0 < t < t_0 + t_s$$

$$i = \frac{V}{R_1} = -\frac{20}{10K\Omega} = -2mA$$



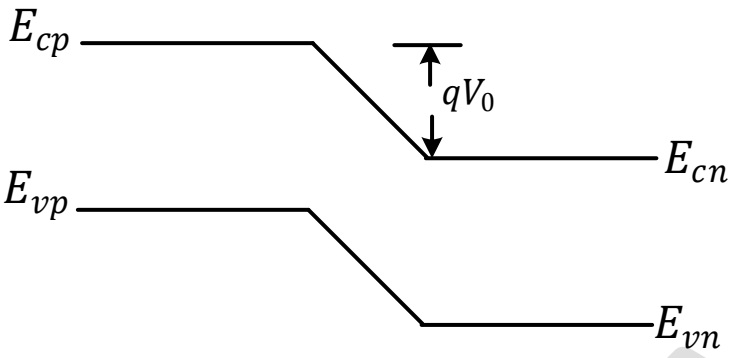
t_s – Storage time is the time for which diode remains in conduction state even in reverse direction

t_t – Transition time is the time taken to return back to non – conduction

8. The built – in potential (Diffusion Potential) in a p – n junction
   (a) Is equal to the difference in the Fermi – level of the two sides, expressed in volts.
   (b) Increases with the increase in the doping levels of the two sides.
   (c) Increases with the increase in temperature.
   (d) Is equal to the average of the Fermi – levels of the two sides.

[GATE 1993: 2 Marks]

Soln. **Contact potential is given by the separation of the energy bands on either side of the junction**

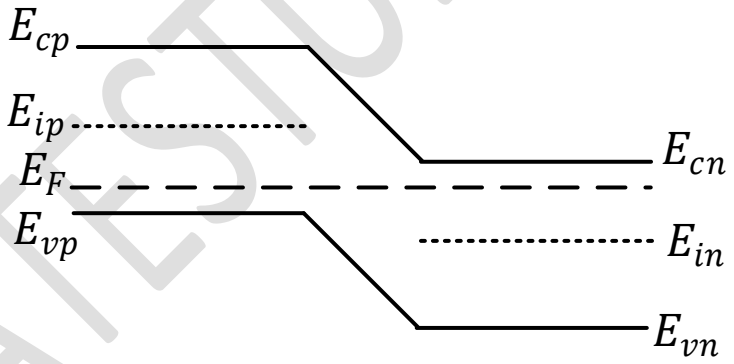


i.e. $\boldsymbol{E_{cp} - E_{vp} = E_{cn} - E_{vn} = q_{v0}}$

It is given by

$$\boldsymbol{V_0 = \frac{kT}{q} \ln\left(\frac{N_a\, N_d}{n_i^2}\right)}$$

Another way to write the contact potential is the difference in Fermi Levels on the two sides of the junction



$$\boldsymbol{V_0 = E_{ip} - E_F + E_F - E_{in}}$$

$$\boldsymbol{= E_{ip} - E_{in}}$$

$$\boldsymbol{= \frac{kT}{q} \ln\left(\frac{N_A}{n_i^2}\right) + \frac{kT}{q} \ln\left(\frac{N_D}{n_i^2}\right)}$$

$$\boldsymbol{V_0 = \frac{kT}{q}\, ln\left(\frac{N_A N_D}{n_i^2}\right)}$$

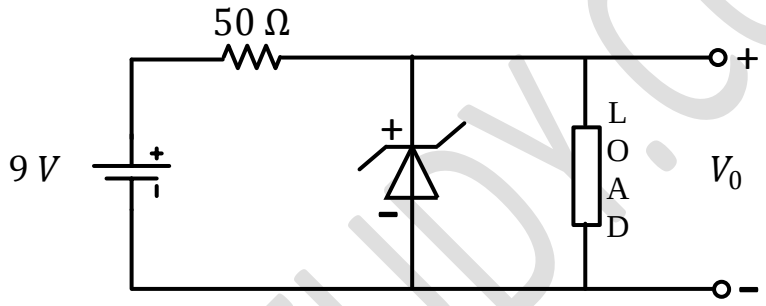
So, as N_A and N_D increase

$$kT \ln\left(\frac{N_A N_D}{n_i^2}\right) \text{ Increases}$$

Thus contact potential (V_0) increases

Options (a) and (b)

9. A Zener diode in the circuit shown in below figure has a knee current of 5mA, and a maximum allowed power dissipation of 300mW. What are the minimum and maximum load currents that can be drawn safely from the circuit, keeping the output voltage V_0 constant at 6V?



(a) 0mA, 180mA
(b) 5mA, 110mA
(c) 10mA, 55mA
(d) 60mA, 180mA

[GATE 1996: 2 Marks]

Soln. Given,

Knee current = 5mA

Maximum power dissipation $\left(P_{D_{max}}\right) = 300mW$

Output voltage $(V_0) = 6V$

Note, Output voltage V_0 is equal to Zener voltage = 6V i.e. $V_0 = V_z$

Max power dissipation of Zener $= I_{z_{max.}} V_z$

$$300mW = 6V \times I_{z\,max}$$

$$or\ I_{z_{max.}} = \frac{300mW}{6} = 50mA.$$

Current through 50 Ω resistor is given by

$$I = \frac{9-6}{50} = \frac{3}{50} = 60mA$$

Minimum and maximum current through load can be obtained as

$$I_{L_{min}} = I - I_{z_{max.}} = 60 - 50 = 10mA$$

$$I_{L_{max}} = I - I_{z_{min.}} = 60 - 5 = 55mA$$

Option (c)

10. A P – N junction in series with a 100 ohms resistor, is forwarded biased. So that a current of 100 mA flows. If the voltage across this combination is instantaneously reversed at t = 0 current through diode is approximately given by

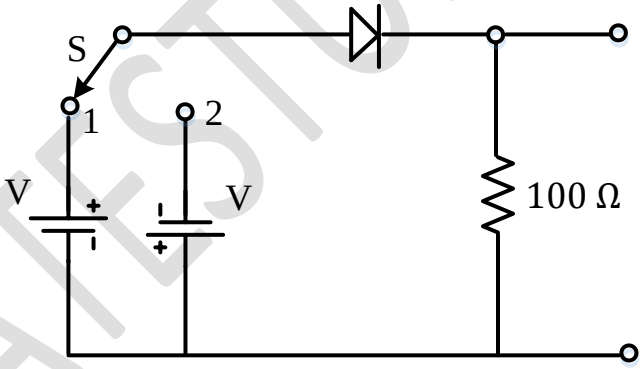
(a) 0 mA (c) 200 mA

(b) 100 mA (d) 50 mA

[GATE 1998: 2 Marks]

Soln. Given,

A P – N junction is in series with 100 ohms resistor P – N junction is basically a diode. The circuit is shown below



Forward current through diode is 100 mA.

$$i.e. \quad \frac{V}{R} = 100\ mA$$

$$or\ V = 100 \times 100mA = 10V$$

Thus, V = 10V

When the voltage is reversed the P – N junction is switched from conduction state. It needs same time to return to non- conduction

state, so the P – N junction behaves as a short circuit for the little time even in reverse direction.

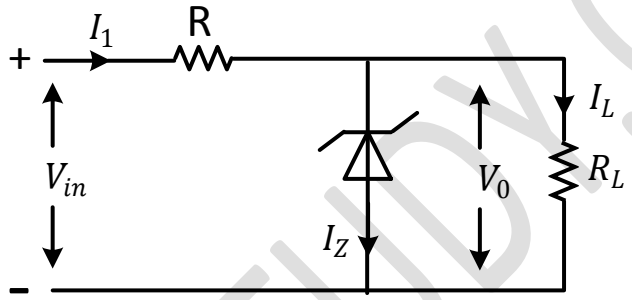
This is due to accumulation of stored access minority charge when diode is forward biased so, the current will be –100 mA

Option (b)

11. A Zener diode regulator in the figure is to be designed to meet the specifications:

$I_L = 10\ mA, V_0 = 10V\ and\ V_{in}$ Varies from 30V to 50V. The Zener diode has $V_Z = 10V$ and I_{ZK} (Knee current) = 1 mA.

For satisfactory operation.



(a) $R \leq 1800\ \Omega$
(b) $2000\ \Omega \leq R \leq 2200\ \Omega$
(c) $3700\ \Omega \leq R \leq 4000\ \Omega$
(d) $R > 4000\ \Omega$

[GATE 2002: 2 Marks]

Soln. Zener diode regulator is to be designed

$$\boldsymbol{I_L = 10\ mA}$$

$$\boldsymbol{V_0 = 10\ V}$$

$$\boldsymbol{V_{in}\ is\ from\ 30\ V\ to\ 50\ V}$$

$$\boldsymbol{V_z = 10\ V\ and\ I_{zk}(Knee\ voltage) = 1\ mA}$$

The current provided by the input circuit should provide load current (I_L) plus Zener current

$$\frac{V_{i\,min} - V_a}{R} \geq I_{z\,min} + I_L$$

When $\boldsymbol{V_{in} = 30\ V}$

$$or,\ \frac{30-10}{R} \geq (10+1)mA$$

$$or,\ \frac{20}{R} \geq 11mA$$

$$or,\ R \leq 1818\Omega \quad ------ (I)$$

When $V_{in} = 50\ V$

$$\frac{50-10}{R} \geq (10+1)mA$$

$$or,\ \frac{40}{R} \geq 11 \times 10^{-3}$$

$$or,\ R \leq 3636 \quad ------ (II)$$

Thus from equation (I) and (II) the value of $R \leq 1818\Omega$

Option (a)

12. At 300^0K for a diode current of 1mA a certain germanium diode requires a forward bias of 0.1435 V. Where a certain silicon diode requires a forward bias of 0.718 V. Under the conditions stated above the closed approximation of the ratio of reverse saturation current in Ge diode to that in silicon diode is

(a) 1
(b) 5
(c) 4×10^3
(d) 8×10^3

[GATE 2003: 2 Marks]

Soln. Given,

Two diodes are given, one of Ge and other of Si having forward current of 1mA. One has to find the reverse saturation current ratios.

Diode current is given by

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

For Ge diode

$$I_{Ge} = I_{0\,Ge}\left(e^{V_G/\eta V_T} - 1\right)$$

And For Si diode

$$I_{Si} = I_{0\,Si}\left(e^{V_s/\eta V_T} - 1\right)$$

Since current is same in both for given forward bias.

$$1mA = I_{0\,Ge}\left(e^{V_G/\eta V_T} - 1\right) = I_{0\,Si}\left(e^{V_s/\eta V_T} - 1\right)$$

$$or, \quad \frac{I_{0\,Ge}}{I_{0\,Si}} = \frac{\left(e^{V_{Ge}/\eta V_T} - 1\right)}{\left(e^{V_{Si}/\eta V_T} - 1\right)} \cong \frac{e^{V_{Ge}/\eta V_T}}{e^{V_{Si}/\eta V_T}}$$

$$= \frac{e^{0.718/2\times 0.026}}{e^{0.1435/1\times 0.026}} \cong 4176$$

$$\cong 4 \times 10^3$$

Option (c)

13. Match items in Group 1 with items in Group 2, most suitably

Group 1

P. LED
Q. Avalanche Photodiode
R. Tunnel diode
S. Laser

Group 2

1. Heavy doping
2. Coherent radiation
3. Spontaneous emission
4. Current gain

	P	Q	R	S
(a)	1	2	4	3
(b)	2	3	1	4
(c)	3	4	1	2
(d)	2	1	4	3

Soln. LED is operated on the principle of spontaneous emission. Avalanche photo diodes operated on Avalanche effect where there is large current gain.

Tunnel diodes have very large doping of both P and N region.

LASER didoes give out coherent radiation

So, Option (c)

14. Choose Proper substitutes for X and Y to make the following statement correct Tunnel diode and Avalanche photodiode are operated in X bias and Y bias respectively.
(a) X : reverse, Y : reverse
(b) X : reverse, Y : forward
(c) X : forward, Y : reverse
(d) X : forward, Y : forward

[GATE 2003: 2 Marks]

Soln. Tunnel diode is always operated is forward bias where it gives negative resistance region.

Light operated devices are operated in reverse bias. Avalanche photo diode operates in reverse bias

Option (c)

15. Consider an abrupt p – n junction. Let V_{bi} be the built in potential of this junction and V_R be the applied reverse bias. If the junction capacitance (C_j) is 1 pF for $V_{bi} + V_R = 1V \; then \; for \; V_{bi} + V_R = 4V, C_j \; will \; be$
(a) 4 pF
(b) 2 pF
(c) 0.25 pF
(d) 0.5 pF

[GATE 2004: 2 Marks]

Soln. For abrupt P – N junction capacitance is given by

$$C_j \propto \frac{1}{\sqrt{V_R}}$$

$$So, \quad C_{j1} = \frac{K}{\sqrt{V_{R_1}}}$$

$$C_{j2} = \frac{K}{\sqrt{V_{R_2}}}$$

$$So, \quad \frac{C_{j1}}{C_{j2}} = \sqrt{\frac{V_{R_2}}{V_{R_1}}}$$

$$\frac{C_{j1}}{C_{j2}} = \sqrt{\frac{4}{1}} = 2$$

$$or, \quad C_{j2} = \frac{C_{j1}}{2} = \frac{1}{2} = 0.5\ pF$$

Thus, option (d)

16. In an abrupt P – N junction, the doping concentrations on the P – side and N – side are $9 \times 16^{16}/cm^3$ *and* $1 \times 10^6/cm^3$ respectively. The P – N junction is reverse biased and the total depletion width is 3 μm. The depletion width on the P – side is
(a) 2.7 μm (c) 2.25 μm
(b) 0.3 μm (d) 0.75 μm

[GATE 2004: 2 Marks]

Soln. **Concentration on p – side** $(N_A) = 9 \times 10^{16}/cm^3$

Concentration on n – side $(N_D) = 1 \times 10^{16}/cm^3$

$$W = W_n + W_p \quad ---------(i)$$

Also $N_D W_n = N_A W_p \quad ---------(ii)$

Find W_P from the above Eqns.

$$N_A W_p = N_D W_n$$

$$= (W - W_p) N_D$$

Or, $W_p(N_A + N_D) = W N_D$

$$or, \quad W_p = \frac{W\ N_D}{N_A + N_D}$$

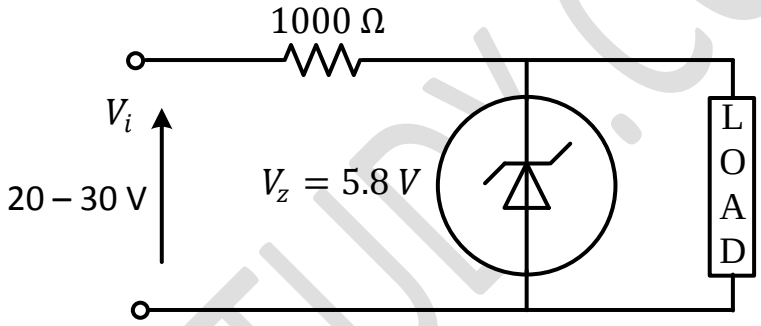
$$= \frac{3 \times 16^{-6} \times 10^{6}}{9 \times 10^{16} + 10^{6}}$$

$$= \frac{3 \times 10^{10}}{10^{17}} = 3 \times 10^{-7}$$

= 0.3 μm

Option (b)

17. The Zener diode in the regulator circuit shown in the figure has Zener voltage of 5.8 volts and a Zener knee current of 0.5 mA The maximum load current drawn from this circuit ensuring proper functioning over the input voltage range between 20 and 30 Voltage, is



(a) 23.7 mA
(b) 14.2 mA
(c) 13.7 mA
(d) 24.2 mA

[GATE 2005: 2 Marks]

Soln. Given,

Zener voltage $(V_z) = 5.8V$

Knee current $(I_{zk}) = 0.5\ mA$

To find the maximum load current that can be drawn from the above circuit.

The maximum load current which can be drawn in the worst case of minimum input voltage and Zener diode current of (I_{zk})**. Source current at the minimum input voltage.**

$$I_s = \frac{V_{in(min)} - V_z}{Rs} = \frac{20 - 5.8}{1\ K} = 14.2\ \text{mA}$$

$$I_L = I_s - I_{z(min)}$$

$$= I_s - I_{zk}$$

$$= 14.2\ mA - 0.5\ mA$$

$$I_L = 13.7\ mA$$

So, I_L will be the maximum load current that can be drawn with minimum input voltage.

Option (c)

18. A Silicon P – N junction under reverse bias has depletion region of width 10 µm. The relative permittivity of silicon, $\varepsilon_r = 11.7$ and the permittivity of free space $\varepsilon_0 = 8.854 \times 10^{-12}\ F/m$. The depletion capacitance of the diode per square meter is

(a) 100 µF (c) 1 µF

(b) 10 µF (d) 20 µF

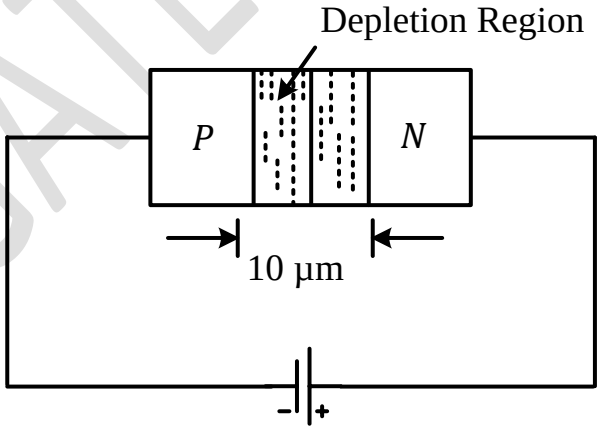
[GATE 2005: 2 Marks]

Soln. Given,

Si P – N junction is Reverse biased

Depletion width = 10 µm.

$$\varepsilon_r\ for\ Si = 11.7$$



Find capacitance per Sq m

When P – N junction is reverse biased it behaves as parallel plate capacitor whose capacitance is given by

$$C = \frac{\varepsilon A}{W}$$

Where, A – Cross section area of junction

W – Thickness of space charge

ε - Dielectric constant

$$C = \frac{\varepsilon_0 \varepsilon_r}{W} A$$

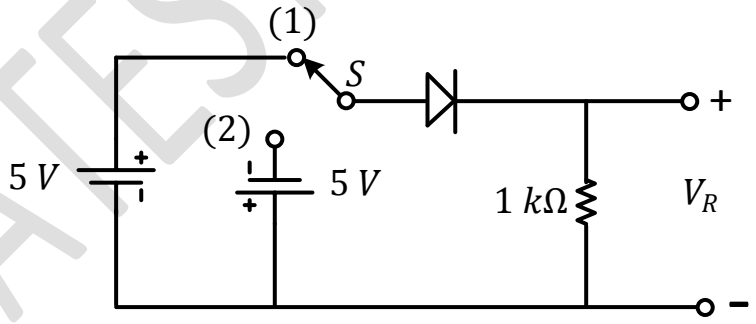
Capacitance per unit area $= \frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{W}$

$$= \frac{11.7 \times 8.54 \times 12^{-12}}{10 \times 10^{-6}}$$

= 10 μF

Option (b)

19. In the circuit shown below, the switch was connected to position 1 at t < 0, is changed to position 2 at t = 0. Assume that the diode has zero voltage drop and a storage time t_s For $0 < t \leq t_s$ V_R is given by (all in volts)



(a) $V_R = -5$
(b) $V_R = 5$
(c) $0 \leq V_R < 5$
(d) $-5 < V_R < 0$

[GATE 2006: 2 Marks]

Soln. Given,

Switch in position 1 for t < 0

Switch to position 2 at t = 0

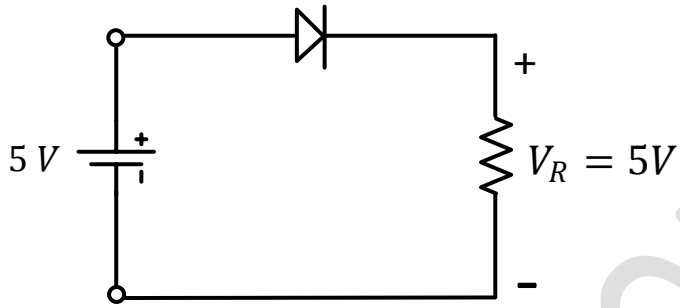
Find V_R for $0 < t \leq t_s$.

When switch at position 1

+5V is applied to diode and diode is forward based

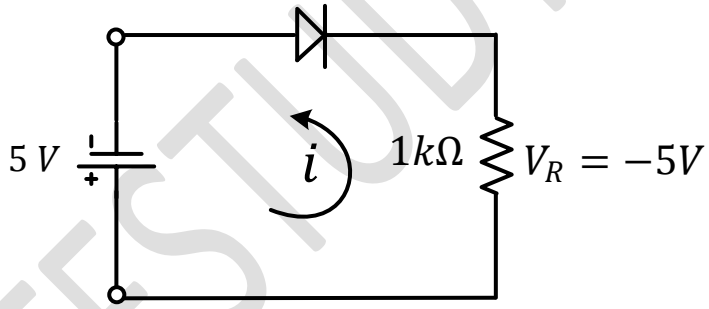
$$V_R = 5V$$

For t < 0



The diode is switched to position 2 (-5V) diode is reverse biased. Diode does not turn to non – conduction immediately but takes some time, so behaves short circuited for small time.

$$for\ 0 < t < t_s$$

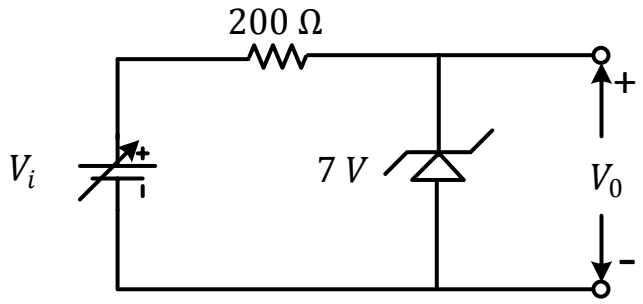


The diode remains in conduction during the storage time t_s and

Output = -5V

Option (a)

20. For the Zener diode shown in the figure, the Zener voltage at knee is 7V, the knee current is negligible and the Zener dynamic resistance in 10Ω. If the input voltage (V_i) range is from 10 to 16V, the output voltage (V_0) range from.



(a) 7.00 to 7.29V
(b) 7.14 to 7.29V
(c) 7.14 to 7.43V
(d) 7.29 to 7.43V

[GATE 2007: 2 Marks]

Soln. Given,

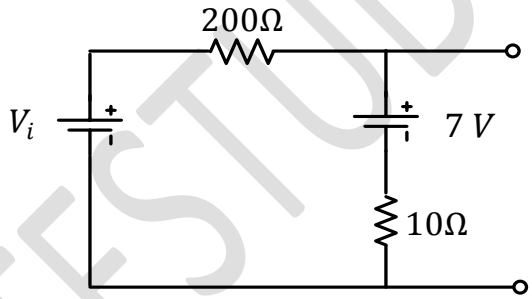
$\boldsymbol{V_z = 7V}$

Zener resistance = 10Ω

V_i is between 10V to 16V

Find the output voltage range

The equivalent circuit is drawn,



when V_i = 10

Current through the circuit $\boldsymbol{I = \frac{10-7}{200+10} = \frac{3}{200} A}$

So, output voltage $\boldsymbol{(V_{01}) = 7 + 10\, I = 7 + 10 \times \frac{3}{210} = 7.14V}$

When V_i = 16V

$$\boldsymbol{I = \frac{16-7}{200+10} = \frac{9}{210} A}$$

$$\boldsymbol{V_{02} = 7 + 10I = 7 + 10 \times \frac{9}{210}}$$

$$\boldsymbol{= 7.43\ V}$$

Option (c)

21. Group I lists four types of P – N junction diodes. Matches each devices in Group – I with one of the options in Group – II to indicate the bias condition of that device in its normal mode of operation

Group – I	**Group – II**
P. Zener diode	1. Forward bias
Q. Solar cell	2. Reverse bias
R. LASER diode	
S. Avalanche photo diode	

Codes

	P	**Q**	**R**	**S**
(a)	1	2	1	2
(b)	2	1	1	2
(c)	2	2	1	1
(d)	2	1	2	2

[GATE 2007: 2 Marks]

Soln. Zener diode operates in reverse bias Avalanche Photodiodes also operate in reverse bias.

Solar cell operate in forward bias but photo current is in reverse direction (3rd quadrant) lease diodes operate is forward bias

Thus Option (b)

22. A P^+ - N junction has built in potential of 0.8V. The depletion layer width at a reverse bias of 1.2V is 2 μm. For a reverse bias of 7.2V, the depletion layer width will be

(a) 4μm (c) 8μm

(b) 4.9μm (d) 12μm

[GATE 2007: 2 Marks]

Soln. Given,

P^+ N junction, $V_{bi} = 0.8V$

Reverse bias = 1.2V, W = 2μm.

Junction potential = Built in potential + reverse bias voltage.

$$V_j = V_0 + V_R$$

For abrupt P^+ N junction depletion width is given by

$$W = \sqrt{\frac{2 \in_s V_{bi}}{qN_D}}$$

$$i.e. \quad W \propto \sqrt{V_{bi}}$$

$$W = K\sqrt{V_{bi}}$$

$$2\mu m = K(0.8 + 1.2)^{1/2} \quad ---------(i)$$

$$x = K(0.8 + 7.2)^{1/2} \quad ---------(ii)$$

From equation (i) and (ii)

So,

$$x = 4\mu m$$

Option (a)

23. Consider the following assertions.
S_1: for Zener effect to occur, a very abrupt junction is required
S_2: for quantum tunnelling to occur, a very narrow energy barrier is required
Which of the following is correct?
(a) Only S_2 is true
(b) S_1 & S_2 both are true but S_2 is not a reason for S_1
(c) S_1 & S_2 both are true but S_2 is a reason for S_1.
(d) Both S_1 & S_2 are false

[GATE 2008: 2 Marks]

Soln. For Zener effect to occur a uniformly doped regions on either side are required.

So, S_1 is not true.

For quantum tunnelling to occur a narrow energy barrier is required.

So, option (a)

24. Compared to a P – N junction with $N_A = N_D = 10^{14}/cm^2$, which one of the following statement is TRUE for a P – N junction with $N_A = N_D = 10^{20}/cm^2$?

(a) Reverse breakdown voltage is lower and depletion capacitance is lower

(b) Reverse breakdown voltage is higher and depletion capacitance is lower

(c) Reverse breakdown voltage is lower and depletion capacitance is higher

(d) Reverse breakdown voltage is higher and depletion capacitance is higher

[GATE 2010: 2 Marks]

Soln. Given,

P – N junction has $N_A = N_D = 10^{14}/cm^2$

When N_A and N_D is increased to 10^{20} / cm^3

Then find the variation in Reverse breakdown and depletion capacitance.

Note that breakdown voltage is related as

$$V_B = \frac{\in E_{max}}{2\, q\, N_B}$$

(Refer : Neaman)

Where N_B is doping in low doped region (n region) of P^+N junction

$V_B \propto \frac{1}{N_B}$ since E_{max} is a slight function of doping

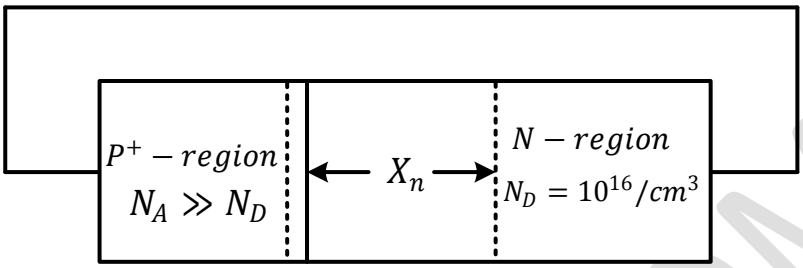
So, as doping increases the value of N_B decreases

Depletion capacitance $(C_T) \propto \frac{1}{W}$ where W is depletion width

So, when doping increases the depletion width decreases so C_T increases

Option (c)

25. Consider an abrupt P^+ N junction (at T = 300 K) shown in the figure. The depletion region width X_n on the N – side of the junction is 0.2 μm and the permittivity of silicon (ε_{si}) is $1.044 \times 10^{-12}\ F/cm$. At the junction, the approximate value of the peak electric field (in k V/cm) is _____



[GATE 2014: 2 Marks]

Soln. Given,

$$N_D = 10^{16}\ /\ cm^3$$

$$N_A \gg N_D \quad since\ Junction\ is\ P^+N$$

Depletion width on n – side = 0.2 μm.

$$\in_{si} = 1.044 \times 10^{-12}\ F/m$$

$$X_n = 0.2\ \mu m$$

For abrupt P^+ N junction Maximum electric filed is given by

$$E_{max} = \frac{q\ N_D\ x_{no}}{\in_s}$$

$$Since\ N_A \gg N_D$$

$$ad\ \ W \cong X_n$$

$$E_{max} = \frac{1.6\times10^{-19}\times10^{16}\times0.2\times10^{-4}}{1.044\times10^{-12}}$$

(Note x_{n0} is given in m)

$$= 30.65 \times 10^3\ V/cm$$

$$E_{max} = 30.65\ Kv/cm$$

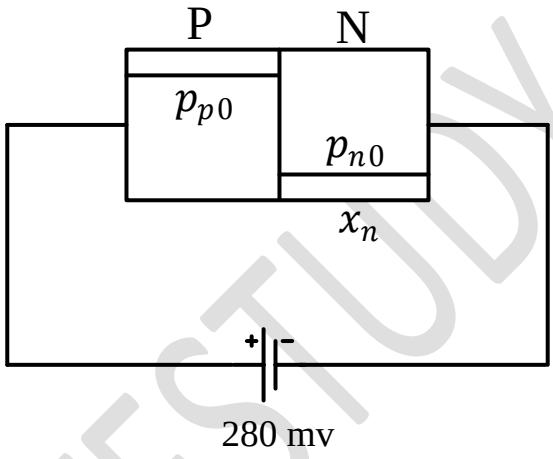
26. For a silicon diode with long P and N regions, the accepter and donor impurity concentrations are $1 \times 10^{17}\ cm^{-3}\ and\ 1 \times 10^{15}\ cm^{-3}$, respectively. The lifetimes of electrons in P region and holes in N region are both 100 μs. The electrons and hole diffusion coefficients are 49 cm^2/s and 36 cm^2/s, respectively. Assume $kT/q = 26mV$, the intrinsic carrier concentration is $1 \times 10^{10}\ cm^{-3}\ and\ q = 1.6 \times 10^{-19}\ C$. When a forward voltage of 208 mV is applied across the diode the hole current density (in nA/cm^2) injected from P region to N region is _____

[GATE 2015: 2 Marks]

Soln. Given,

Acceptor impurity concentration $(N_A) = 1 \times 10^{17}/cm^3$

Donor impurity concertation $(N_D) = 1 \times 10^{15}/cm^3$



Life time of minority carriers in P and N region = 100 μs

Diffusion coefficients $= (D_n) = 49\ cm^2/S$

Diffusion coefficients $= (D_p) = 36\ cm^2/S$

Intrinsic concentration $(n_i) = 1 \times 10^{10}/cm^3$

Forward bias = 280 mV

Hole current density injected from P region to N region can be given as

$$J_{p(x_n)} = \frac{q\,D_p\,n_i^2}{N_D\,L_p}\left(e^{V/V_T} - 1\right)$$

Where, D_p– Diffusion coefficients

p_{n0} **− hole concertation on n side in equilibrium.**

L_p **− Diffusion length of holes**

$$J_{pn(x_n)} = \frac{q\,D_p}{\sqrt{D_p\,\tau_P}}\,p_{n0}\left(e^{V/V_T} - 1\right)$$

$$= \frac{1.6 \times 10^{-19} \times 36}{\sqrt{36 \times 100 \times 10^{-6}}} \times 1 \times 10^5 \left(e^{0.28/0.026} - 1\right)$$

$$Since \quad p_{no} = \frac{n_1^2}{n_{p0}} = \frac{10^{20}}{10^{15}} = 10^5$$

$$= 2.861 \times 10^{-8}\ A/cm^2$$

$$= 28.61 \times 10^{-9}\ A/cm^2$$

$$J_{p(x_n)} = 2.861 \times 10^{-8}\ nA/cm^2$$

Answer . $28.61 \times 10^{-8}\ nA/cm^2$

27. The built in potential of an abrupt P – N junction is 0.75 V. If its junction capacitance (C_J) at a reverse bias (V_R) of 1.25 V *is* 5 pF, the value of C_J $(in\ pF)$ when $V_R = 7.25\ V$ is ___

[GATE 2015: 2 Marks]

Soln. Given,

Built potential $(V_{bi}) = 0.75\ V$

$C_j = 5pt\ when\ V_R = 1.25V$

C_j =? $when\ V_R = 7.25V$

For an abrupt P – N junction

$$C_j = \frac{K}{\sqrt{V_j}} = \frac{K}{\sqrt{V_0 + V_R}}$$

$$\frac{C_{j2}}{C_{j1}} = \frac{\sqrt{V_0 + V_{R1}}}{\sqrt{V_0 + V_{R2}}}$$

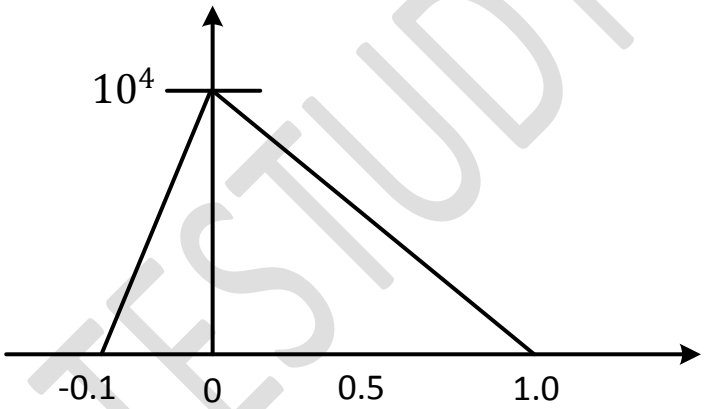
$$or \quad \frac{C_{j2}}{C_{j1}} = \frac{\sqrt{0.75 + 1.25}}{\sqrt{0.75 + 7.25}}$$

$$or, \quad C_{j2} = \frac{1}{2} C_{j1}$$

$$or, \quad C_{j2} = \frac{1}{2} \times 5pF = 2.5pF$$

Answer 2.5pF

28. The electric field profile in the depletion region of a P – N junction in equilibrium is shown in the figure. Which one of the following statements is NOT TRUE?



(a) The left side of the junction is n – type and the right side is p – type
(b) Both the n – type and p – type depletion region are uniformly doped
(c) The potential difference across the depletion region is 700 mV
(d) If the p – type region has a doping concentration of 10^{15} cm^{-3} then the doping concentration in the n – type region will be 10^{16} cm^{-3}

[GATE 2015: 2 Marks]

Soln. As per option (c) we try to find the potential across the depletion region.

This can be done by finding the area of the given field variation

i.e. Built in potation $= \frac{1}{2} \times (1.1 \times 10^{-6}) \times 10^6 \; v/m$

= 0.55 volts

But in the option it is given 0.7 u

So, the option is (c) which is not true

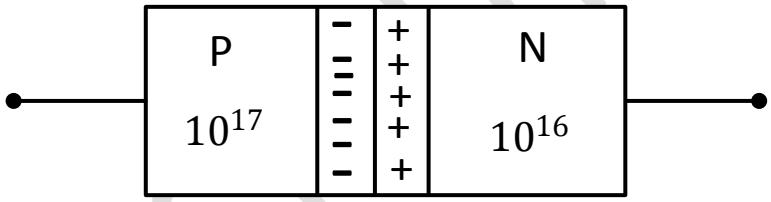
29. Consider a silicon P – N junction with a uniform acceptor doping concentration of 10^{17} cm^{-3} on the P – side and a uniform donor doping concentration of 10^{6} cm^{-3} on the N – side. No external voltage is applied to the diode

Given: $\frac{kT}{q} = 26\ mV, n_i = 1.5 \times 10^{10}\ cm^{-3}, \varepsilon_{si} = 12\varepsilon_0, \varepsilon_0 = 8.85 \times 10^{-14}\frac{F}{m}, and\ q = 1.6 \times 10^{-19} C.$

The charge per unit junction area (nC cm^{-2}) in the depletion region on the P – side is _____

[GATE 2016: 2 Marks]

Soln. Given,



$$\frac{kT}{q} = 26\ mV$$

$$n_i = 1.5 \times 10^{10}/cm^3$$

$$\in_{si} = 12 \in_0 \quad , \quad \in_0 = 8.854 \times 10^{-14}\ F/m$$

$$q = 1.6 \times 10^{-19}\ C$$

$$\in = 12\ \in_0 = 12 \times 8.85 \times 10^{-4}\ F/m$$

$$N_D = 10^{16}\ cm^{-3} = 10^{22}\ m^{-3}$$

$$N_A = 10^{17}\ cm^{-3} = 10^{23}\ m^{-3}$$

Built in potential $(V_0) = \frac{kT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right]$

$$= 0.026 \ln\left[\frac{10^{23}\times 10^{22}}{(1.5\times 10^{16})^2}\right]$$

$$V_0 = 0.757\ V$$

$$W = \sqrt{\frac{2\in}{q} V_0 \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}$$

$$= \sqrt{\frac{2\times 12\times 8.854\times 10^{-14}}{1.6\times 19^{-19}}} \times 0.75 \left(\frac{1}{10^{23}} + \frac{1}{10^{22}}\right)$$

$$3.325 \times 10^{-8}\ m$$

$$W = 3.325 \times 10^{-6}\ cm$$

$$W_p = \frac{N_D}{N_A + N_D} . W = \frac{10^{22}}{10^{22}+10^{23}} \times 3.325 \times 10^{-8}$$

$$= 3.023 \times 10^{-9}\ m \quad = \quad 3.023 \times 10^{-7}\ cm$$

Charge (Q) = W_P N_A q . A

$$or \quad \frac{Q}{A} = W_P\ N_A\ q$$

$$= 3.023 \times 10^{-7} \times 10^{17} \times 1.6 \times 10^{-19}$$

$$4.836 \times 10^{-9}\ cm^{-2}$$

In depletion region on p – side negatively charged acceptor ions exist. Here charge per unit area ($n\ C\ cm^{-2}$) in depletion region on the p – side is

$$-4.836\ n\ C\ cm^{-2}$$

30. Consider avalanche breakdown in a silicon p^+ n junction. The n – region is uniformly doped with a donor density N_D. Assume that breakdown occurs when the magnitude of the electric field at any point in the device becomes equal to the critical filed E_{crit} . Assume E_{crit} to be independent of N_D. If the built – in voltage of the p^+ n junction is much smaller than the breakdown voltage, V_{BR}, the relationship between V_{BR} and N_D is given by

(a) $V_{BR} \times \sqrt{N_D} = constant$
(b) $N_D \times \sqrt{V_{BR}} = constant$
(c) $V_{BR} \times N_D = constant$
(d) $N_D / V_{BR} = constant$

[GATE 2016: 2 Marks]

Soln. The breakdown voltage can be calculated from the critical field for one sided abrupt junction (P^+N)

Breakdown voltage

$$= \left(V_{BR} = \frac{\in_S E_{crit}^2}{2q} \right) . \frac{1}{N_B}$$

Where $N_B = N_D$

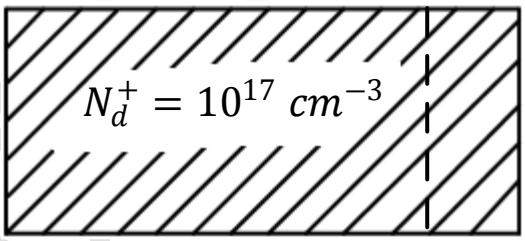
So,

$$V_{BR} = \frac{\in_S E_{crit}^2}{2q} . \frac{1}{N_B}$$

$$Or, \quad V_{BR} . N_D = \frac{\in_S E_{crit}^2}{2q} = A\ constent$$

Option (c)

31. Consider a region of silicon devoid of electrons and holes, with an ionized donor density of $N_d^+ = 10^{17}\ cm^{-3}$. The electric at $x = 0\ is\ 0\ V/cm$ and the positive x direction. Assume that the electric filed is zero in the y and z directions al all points.



Given $q = 1.6 \times 10^{-19}\ coulomb, \in_0 = 8.85 \times 10^{-14}\ \frac{F}{cm}$ $\in_0 = 11.7$ for silicon, the value of L in nm is _____.

[GATE 2016: 2 Marks]

Soln. Given,

Ionised donor density is given

$$N_d^+ = 10^{17}/cm^3$$

Using Poisson's equation

$$\frac{dE}{dx} = \frac{q \,.\, N_D}{\in}$$

$$or, \quad \frac{50\ kV/cm - 0}{L - 0} = \frac{1.6 \times 10^{-19} \times 10^{17}}{11.7 \times 8.854 \times 10^{-14}}$$

$$= 3.2358 \times 10^{-8}\ m$$

$$L = 32.358\ nm$$

32. The I – V characteristics of the Zener diodes D1 and D2 are shown in Figure I. These diodes are used in the circuit given in Figure II. If the supply voltage is varied from 0 to 100 V, then breakdown occurs in

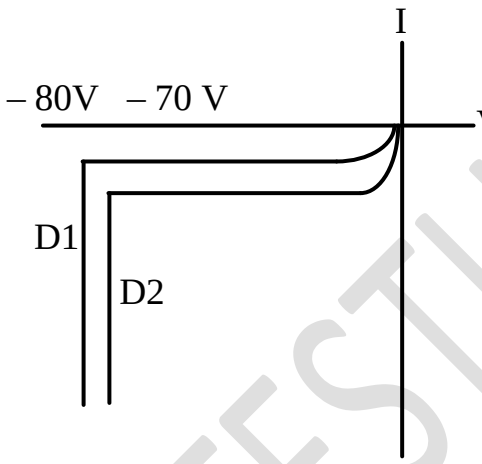


Figure I

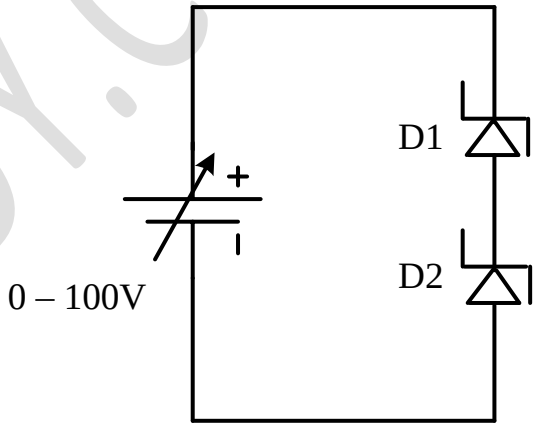


Figure II

(a) D1 only
(b) D2 only
(c) Both D1 and D2
(d) None of D1 and D2

[GATE 2016: 2 Marks]

Soln. In the given circuit (figure II) D_1 and D_2 are Zener diode connected in series

D_2 has Zener voltage of –70 V while D_1 has Zener voltage of –80 V supply voltage is varied from 0 to 100V. The polarity of the voltage is to reverse bias the diodes.

For Zener diode to go to breakdown following conditions be satisfied.

(i) Current through diode should be more than knee current (I_{zk})
(ii) Voltage across diode is equal to V_z

As the supply voltage is increased from 0 V towards 100 V

Initially both diodes are reverse biased when the voltage is increased

Note that reverse current of diode D_1 is less than of diode D_2

Hence when V_{in} is greater than 80V D_1 goes to breakdown (since its current is lower) and D_2 is not in breakdown. When D_1 goes to breakdown the current flows. The current through the circuit may be equal to or more than that as required by D_2.

But since the reverse voltage of D_2 is less than breakdown voltage, it will not go into Zener region.

Option (a)