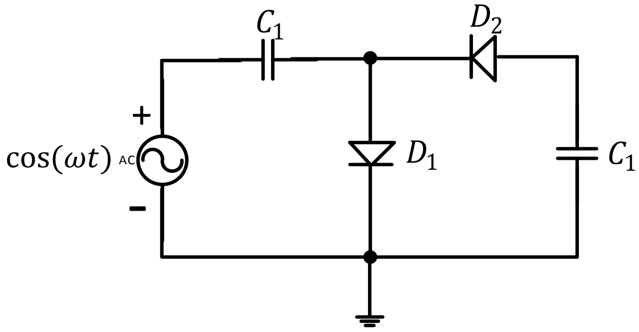
# Diode Circuits – Recent GATE Problems

1. The diodes and capacitors in the circuit shown are ideal. The voltage v(t) across the diode $D_1$ is




(a) $\cos(\omega t) - 1$ (c) $1 - \cos(\omega t)$
(b) $\sin(\omega t)$ (d) $1 - \sin(\omega t)$

**[GATE 2012: 1 Mark]**

**Soln. Given,**

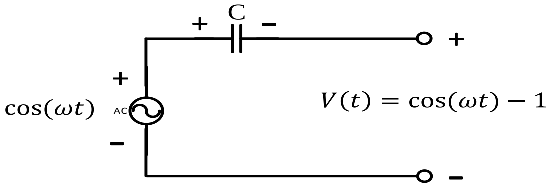
**Voltage $v(t) = \cos \omega t$**

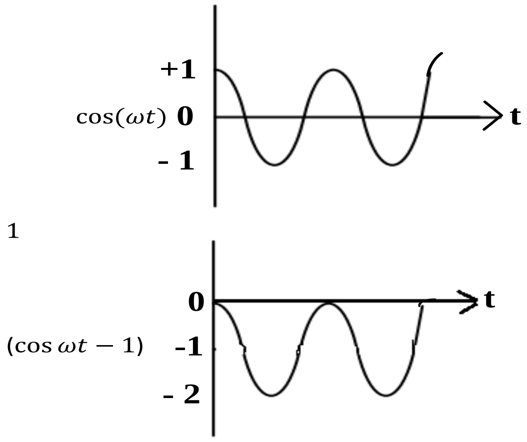
**Find the voltage across the diode $D_1$ (diodes and capacitors are ideal) When the positive cycle of the input is applied diode $D_1$ is forward biased and $D_2$ is reverse biased.**

**Capacitor $C_1$ charges to maximum voltage (here 1 V)**

**When negative cycle of the input comes $D_1$ is reverse biased, so replaced by open.**

**Note that $D_2$ is reverse biased forever and can be replaced by a open switch.**



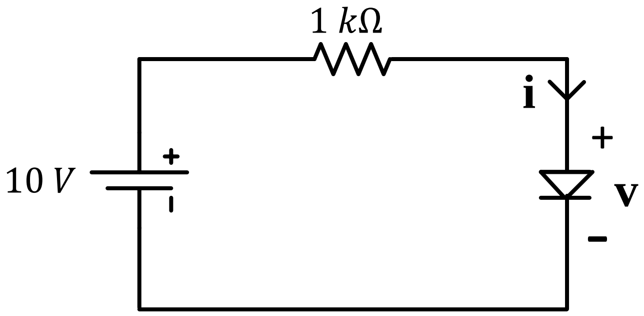



**In this circuit $C_1$ & $D_1$ form a clamper circuit while $D_2$ and $C_2$ form peak detector. This cascaded circuit acts as peak to peak detector.**

**Option (a)**

2. The i – v characteristics of the diode in the circuit given below are

$$i = \begin{cases} \frac{v-0.7}{500} A, & v \geq 0.7\,V \\ 0A, & v \geq 0.7\,V \end{cases}$$




The current in the circuit is

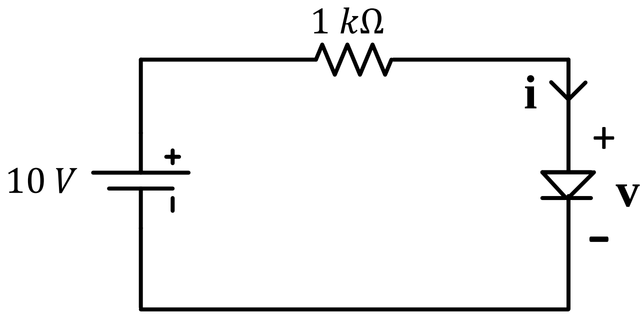
(a) 10 mA
(b) 9.3 mA
(c) 6.67 mA
(d) 6.2 mA

**[GATE 2012: 1 Mark]**

**Soln. As per the given i – v characteristics**

$$\boldsymbol{i = \frac{v-0.7}{500}\ A\ for\ v \geq 0.7\ V - - - - - - - - - - - (1)}$$

**From the given circuit,** $\boldsymbol{v = 10 - 1000i - - - - - (2)}$



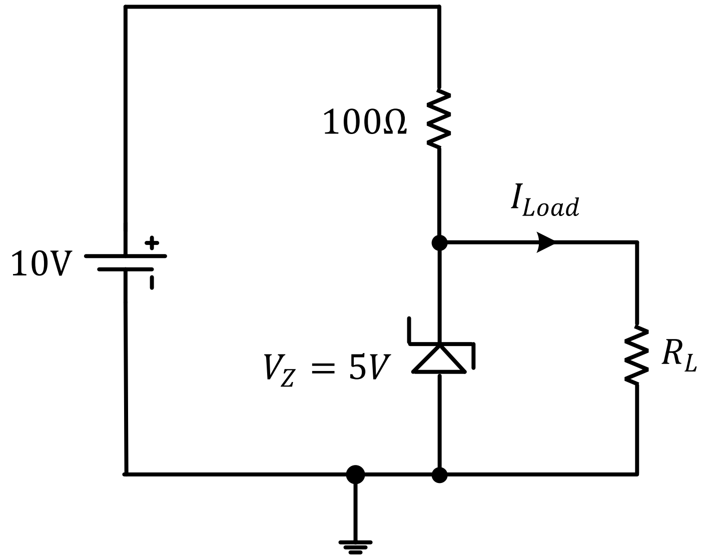

**From equation (1) and (2) eliminate v**

$$\boldsymbol{i = \frac{10 - 1000i - 0.7}{500} = \frac{9.3}{500} - 2i}$$

$$or,\quad 3i = \frac{9.3}{500} \quad or \quad i = \frac{3.1}{500} = 6.2mA$$

**Thus, option (d)**

3. In the circuit shown below, the knee current of the ideal Zener diode is 10 mA. To maintain 5 V across $R_L$, the minimum value of $R_L$ in Ω and the minimum power rating of the Zener diode in mW, respectively are




(a) 125 and 125
(b) 125 and 250
(c) 250 and 125
(d) 250 and 250

**[GATE 2013: 2 Marks]**

**Soln. Given,**

**Knee current of Zener** $(I_{zk}) = 10mA$

**Knee current of Zener is the minimum current that should flow through the diode for proper Zener action**

**Zener is of 5V i.e.** $V_z = 5V$

**Find, minimum $R_L$ and diode power rating.**

**The minimum value of $R_L$ means the load current is maximum ($I_{max}$)**

**So,**

$$V_{RL} = I_{Lmax} \cdot R_{min}$$

$$or,\quad R_{min} = \frac{V_{RL}}{I_{Lmax}} = \frac{5}{I_{Lmax}} \quad ------(1)$$

**Note,**

$$I = I_{zk} + I_{Lmax}$$

$$or, \quad I_{Lmax} = I - I_{zk} = 50 - 10 = 40mA$$

$$R_{min} = \frac{5}{40 \times 10^{-3}} = \frac{5000}{40} = \frac{500}{4} = 125\Omega$$

**Minimum power rating of Zener diode.**

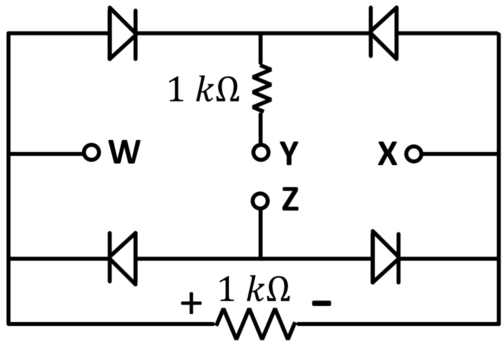
**It will be decided by the maximum current in Zener.**

$$P_z = V_z \, . I_{zmax}$$

$$= 5 \times 50\ mA = 250\ mW$$

**Option (b)**

4. A voltage 1000 $\sin(\omega t)$ volts is applied across YZ. Assuming ideal diodes, the voltage measured across WX in volts, is




(a) $\sin(\omega t)$
(b) $(\sin \omega t + |\sin \omega t|)/2$
(c) $(\sin \omega t - |\sin \omega t|)/2$
(d) 0 for all t

**[GATE 2013: 2 Marks]**

**Soln.** **Voltage applied across Y – Z terminals** $v_i = 1000\ sin\ \omega t$

**Diodes are assumed ideal**

**For positive cycle of the input**

**All four diodes are Reverse biased**

$$V_W - V_X = 0$$

$$or, \quad V_{WX} = 0$$

**For negative cycle of the input**

**All diodes are forward biased i.e. short circuited**

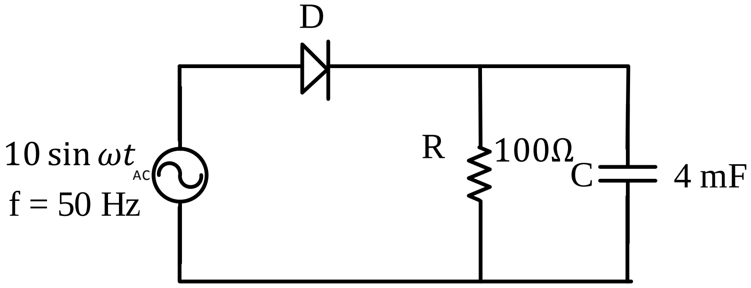
$$V_{WX} = V_W - V_X = 0$$

**Thus,**

**$V_{WX}$ is zero for all times**

**Option (d)**

5. The figure shows a half-wave rectifier. The diode D is ideal. The average steady-state current (in Amperes) through the diode is approximately ___




**[GATE 2014: 1 Mark]**

**Soln. Given,**

**Input signal = $10\ sin\ \omega t$**

**Frequency = 50 Hz**

**Period of the waveform $T = \frac{1}{f} = \frac{1}{50} = 20\ m\ sec$**

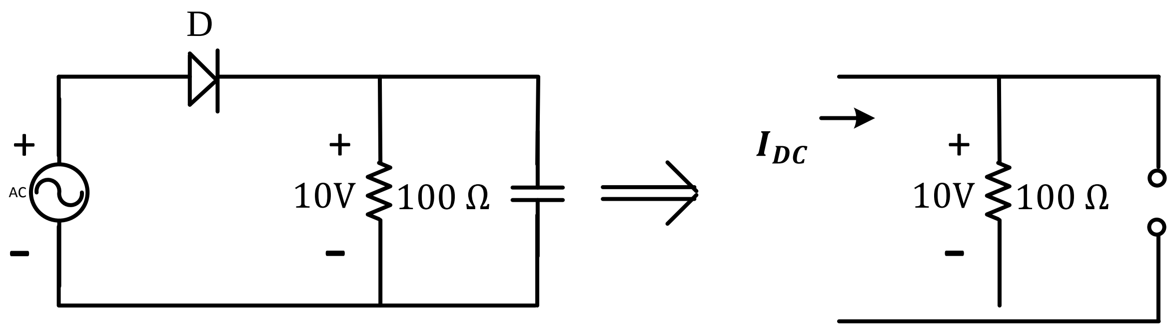
**Time constant = $RC = 100 \times 4 \times 10^{-3}\ sec.$**

**= 400 m sec.**

**Note here,**

**RC >> T**

**Thus the voltage across the resistor can be approximated to 10V (DC).**




**Current through the diode**

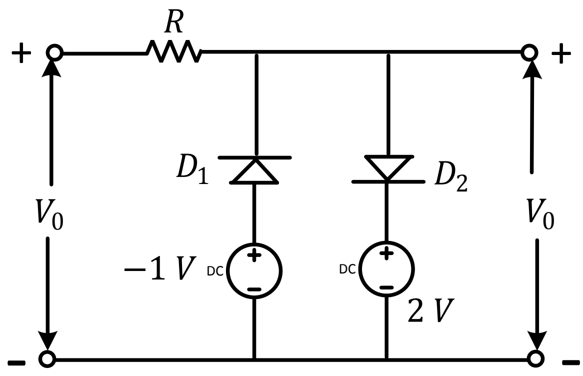
$$I_D(DC) = \frac{10V}{100} = 0.1\ A$$

**This circuit is also sometimes called half wave peak detector. In AM receives it is used to detect envelope of AM wave**

**Answer 0.1 A**

6. Two silicon diodes, with a forward voltage drop of 0.7 V, are used in the circuit shown in the figure. The range of input voltage $V_i$ for which the output voltage $V_0 = V_i$ is

(a) $-0.3\ V < V_i < 1.3\ V$
(b) $-0.3\ V < V_i < 2\ V$
(c) $-1.0\ V < V_i < 2.0\ V$
(d) $-1.7\ V < V_i < 2.7\ V$




**[GATE 2014: 1 Mark]**

**Soln. Given,**

**Forward voltage drop of the given Si diodes is 0.7V**

**Find, the range of Vi for which output voltage $V_0 = V_i$**

**Let us see the $D_2$ branch of the circuit.**

**$D_2$ will be forward biased when $V_i > 0.7 + 2 = 2.7V$**

D$_2$ will be Reverse biased when $V_i < 2.7V$

**See the branch D$_1$**

**D$_1$ will be forward biased when $V_i < -1 - 0.7 = 1.7V$**

**D$_1$ will be Reverse biased when $V_i > -1.7\ V$**

**When both the diodes will be Reverse biased (both shunt branches will be open) then $V_0 = V_{in}$**

**Thus, it will happen when**

**D$_2$ is Reverse biased i.e. $V_i < 2.7V$**

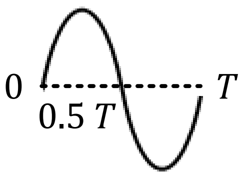
**D$_1$ is Reverse biased i.e. $V_i > -1.7V$**

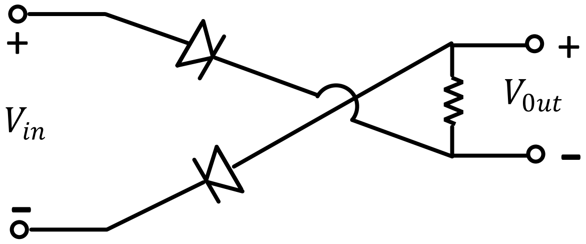
**Thus,**

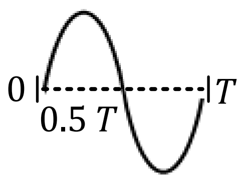
$$-1.7V < V_i < 2.7V$$

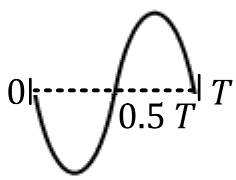
**Option (d)**

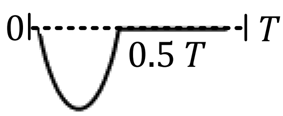
7. For the circuit with ideal diodes shown in the figure, the shape of the output ($V_{out}$) for the given sine wave input ($V_{in}$) will be

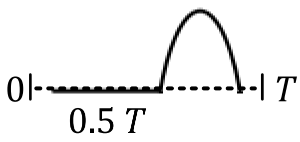



(a)


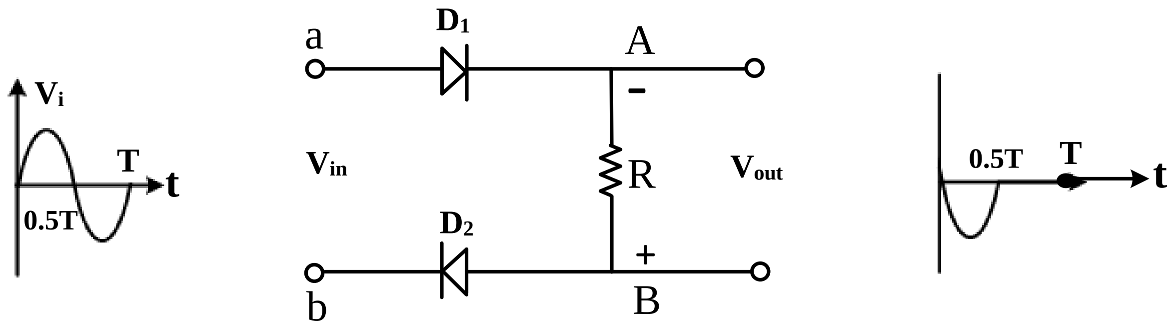

(b)



(c)



(d)



**[GATE 2015: Mark]**

**Soln. The given circuit can be redrawn as**




**For +ve half cycle of the input**

**$D_1$ and $D_2$ are ON**

$$\boldsymbol{V_{out} = -V_{in}}$$

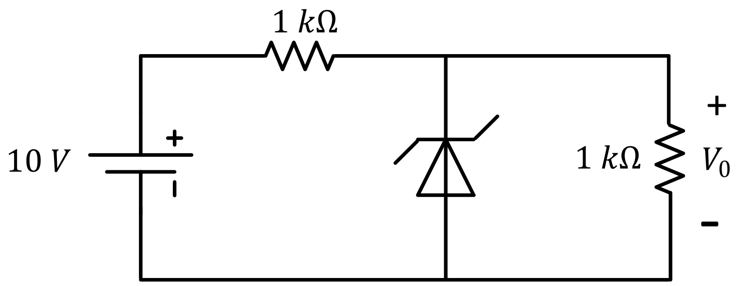
**For –ve half cycle of the input**

**$D_1$ and $D_2$ are off**

$$\boldsymbol{V_{out} = 0V}$$

**Option (c)**

8. In the circuit shown below, the Zener diode is ideal and Zener voltage is 6 V. The output voltage $V_0$ (in volts) is __________.




**[GATE 2015: 1 Mark]**

**Soln. Given,**

**Zener voltage = 6 V**

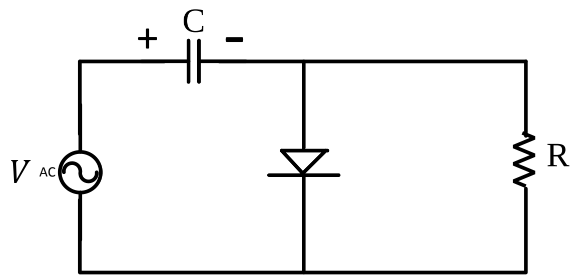
**Zener diode is reverse biased during its operation. Here with the applied voltage, the voltage across the Zener diode is**

$$\boldsymbol{V_0 = \frac{1\,K\Omega}{1K + 1\,K\Omega} \times 10V = 5V}$$

**Diode will be reverse biased but not in the Zener region, so open circuited.**

**Answer Thus, $V_0$ = 5V**

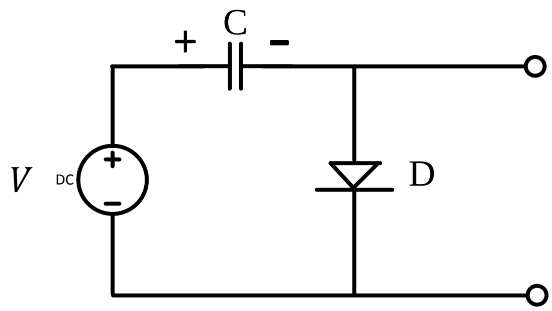
9. If the circuit shown has to function as a clamping circuit, then which one of the following conditions should be satisfied for the sinusoidal signal of period T?




(a) RC << T
(b) RC = 0.35 T
(c) RC = T
(d) RC >> T

**[GATE 2015: 1 Mark]**

**Soln. Observe the following circuit**




**This circuit is of a negative clamper.**

**The present circuit has a load resistor connected in shunt.**

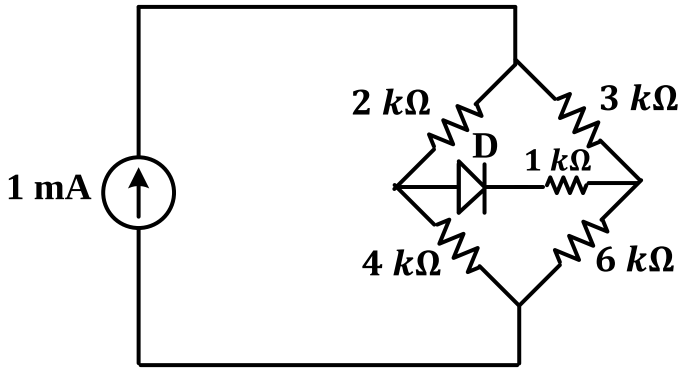
**When diode is off the capacitor discharges through resistor R. The output falls exponentially with time constant RC to avoid the discharge of capacitor significantly**

**RC >> T**

**Where T is period of the sinusoidal waveform applied to the given circuit.**

**Option (d)**

10. The diode in the circuit given below has $V_{ON} = 0.7\ V$ but ideal otherwise. The current (in mA) in the 4 kΩ resistor is ______.




**[GATE 2015: 2 Marks]**

**Soln. The given circuit is a bridge circuit note that the cross arm product is same i.e.**

$$\mathbf{2 \times 6 = 4 \times 3}$$

$$\mathbf{12 = 12}$$

**So, bridge is balanced**

**So no current through 1 kΩ resistor**

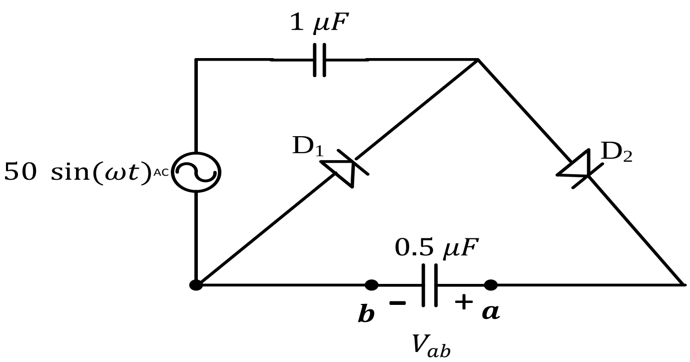
**Now current through 4 kΩ resistor will be**

$$\boldsymbol{I = \frac{9}{9+6} \times 1mA}$$

$$\boldsymbol{= \frac{9}{15} mA = 0.6\ mA}$$

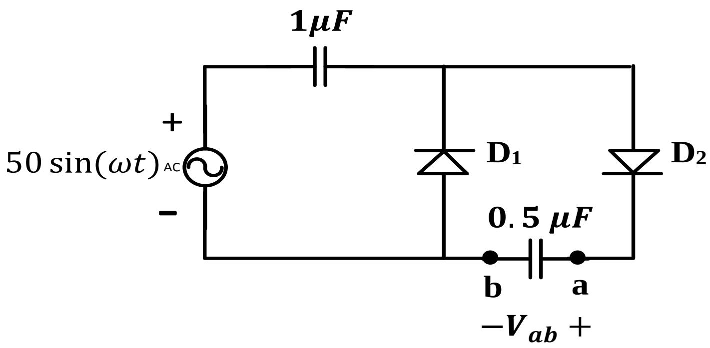
**Answer 0.6 mA**

11. In the circuit shown, assume that diodes $D_1$ and $D_2$ are ideal. In the steady-state condition the average voltage $V_{ab}$ (in Volts) across the 0.5 μF capacitor is _______.




**[GATE 2015: 1 Mark]**

**Soln. The given circuit can be redrawn as follows:**



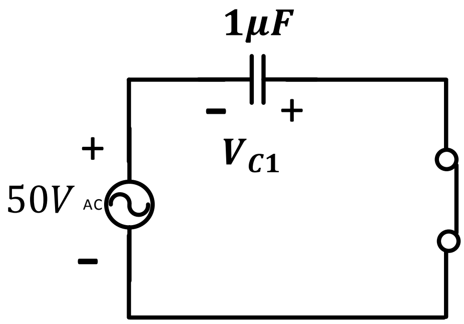

**During –ve half cycle of the applied sinewave input**

**$D_1$ is forward biased**

**Applying KVL**

$$-50 + V_{C1} = 0$$

$$or,\ V_{C1} = 50V$$

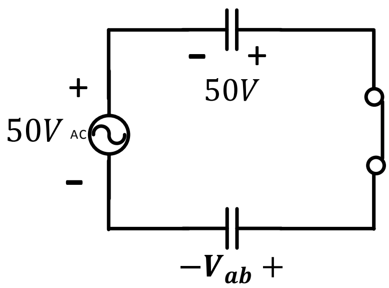



**During +ve cycle of input**

**Applying KVL**

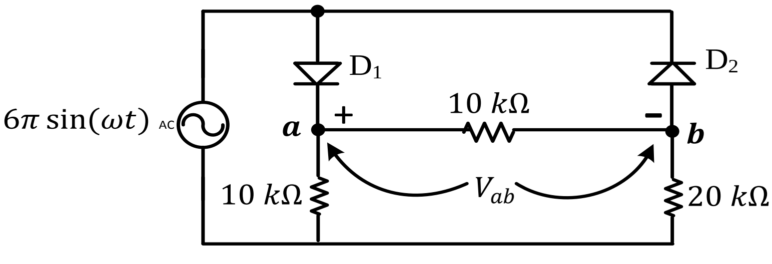
$$50 + 50 - V_{ab} = 0$$

$$or,\ V_{ab} = 100V$$




**Answer 100V**

12. In the circuit shown, assume that the diodes $D_1$ and $D_2$ are ideal. The average value of voltage $V_{ab}$ (in volts) across terminals ‘a’ and ‘b’ is ___.




**[GATE 2015: 1 Mark]**

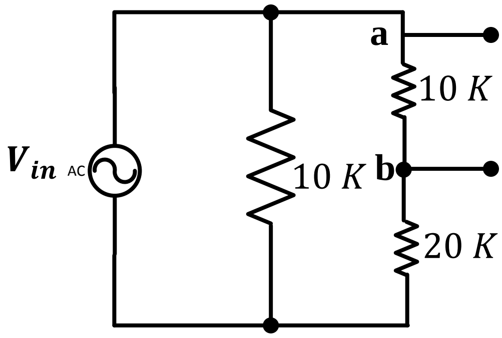
**Soln.** **During positive cycle of the input**

**$D_1$ is Forward biased and**

**$D_2$ is Reverse biased**

**The circuit reduces to**

$$V_{in} = 6\pi \sin \omega t$$




$$V_{ab} = \frac{10\ K}{10\ K + 20\ K} \cdot V_{in}$$

$$= \frac{V_{in}}{3} = \frac{6\pi \sin \omega t}{3} = 2\pi \sin \omega t$$

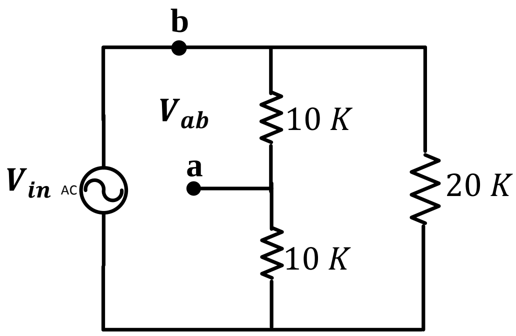
**During negative cycle of the input**

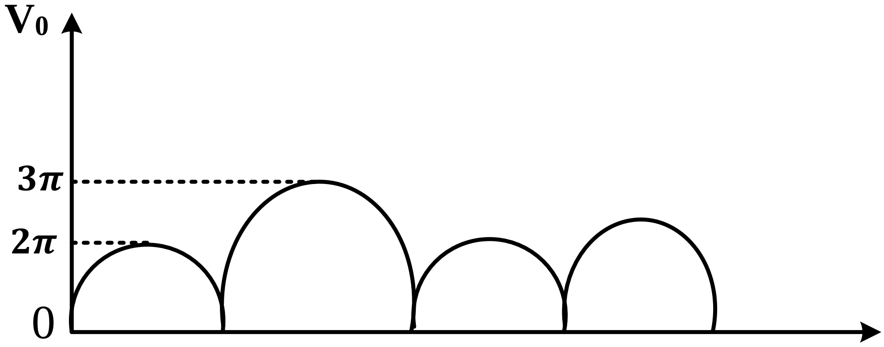
**$D_1$ is Reverse biased**

**$D_2$ is Forward biased**

$$V_{ab} = \frac{10K}{10K + 10K} \cdot V_{in} = {V_{in}}/{2}$$

$$= \frac{6\pi \sin \omega t}{2} = 3\pi \sin \omega t$$

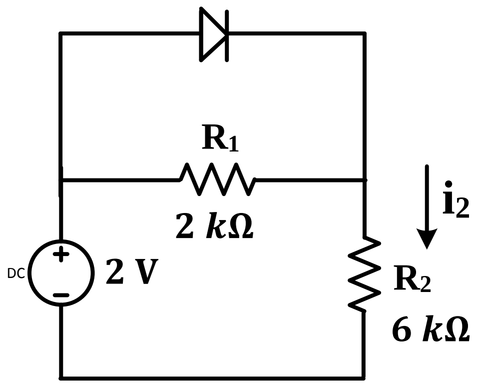


$$V_{ab} = \frac{2\pi}{\pi} + \frac{3\pi}{\pi} = 5\ volts$$

**Answer: 5 volts**

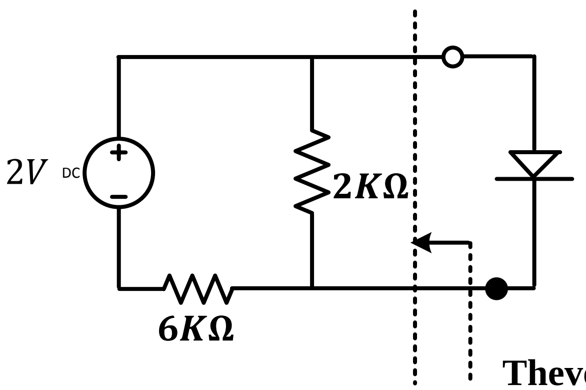
13. Assume that the diode in the figure has $V_{on} = 0.7\ V$, but is otherwise ideal.



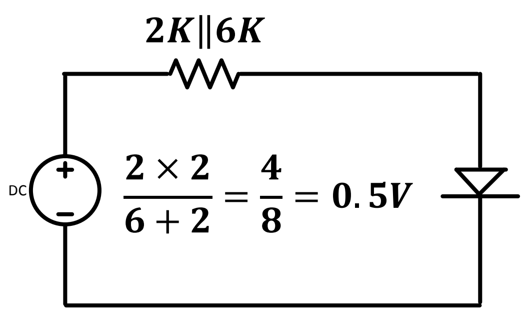

The magnitude of the current $i_2$ (in mA) is equal to ________

**[GATE 2016: 1 Mark]**

**Soln. The given circuit can be redrawn as**

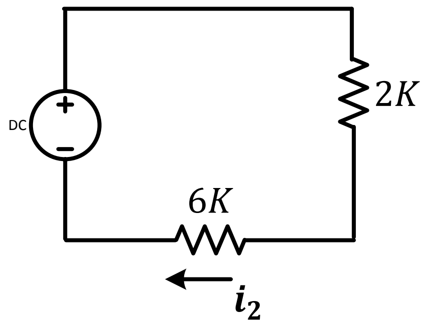



**This circuit can be further simplified using Thevenins theorem**




$$\frac{2 \times 2}{6+2} = \frac{4}{8} = 0.5V$$

**Voltage across diode is 0.5V thus the diode is OFF. The circuit reduces to**

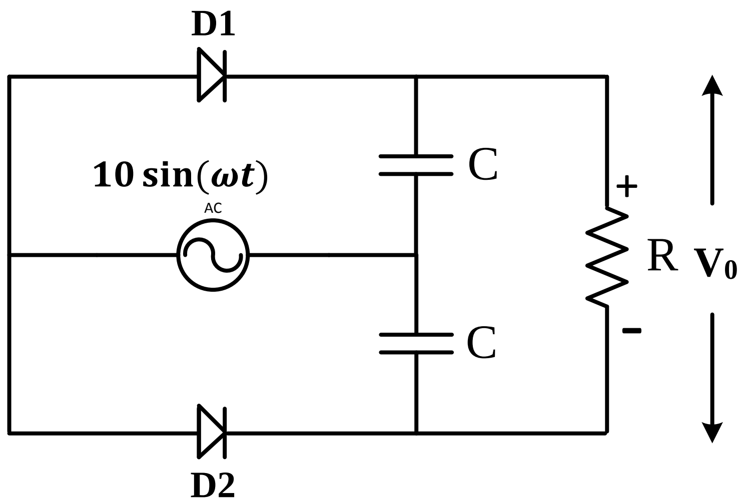



**The current through 6 K**

$$i_2 = \frac{2}{2K + 6K} = \frac{2}{8K} = 0.25\ mA$$

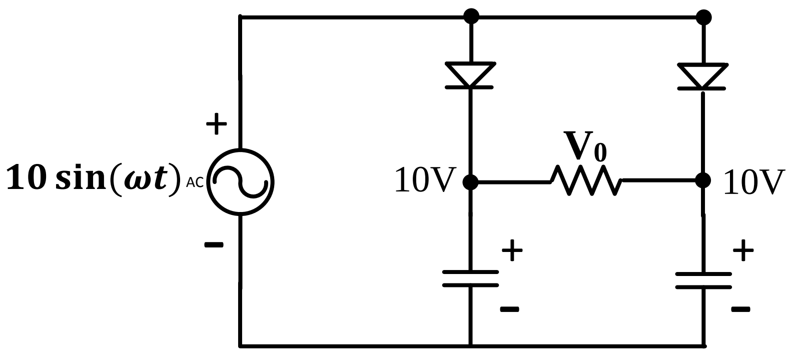
**Answer: 0.25 mA**

14. The diodes D1 and D2 in the figure are ideal and the capacitors are identical. The product RC is very large compared to the time period of the ac voltage. Assuming that the diodes do not breakdown in the reverse bias, the output voltage $V_0$ (in volt) at the steady state is ___________




**[GATE 2016: 1 Mark]**

**Soln. Diodes $D_1$ and $D_2$ are ideal. The above circuit can be redrawn as**



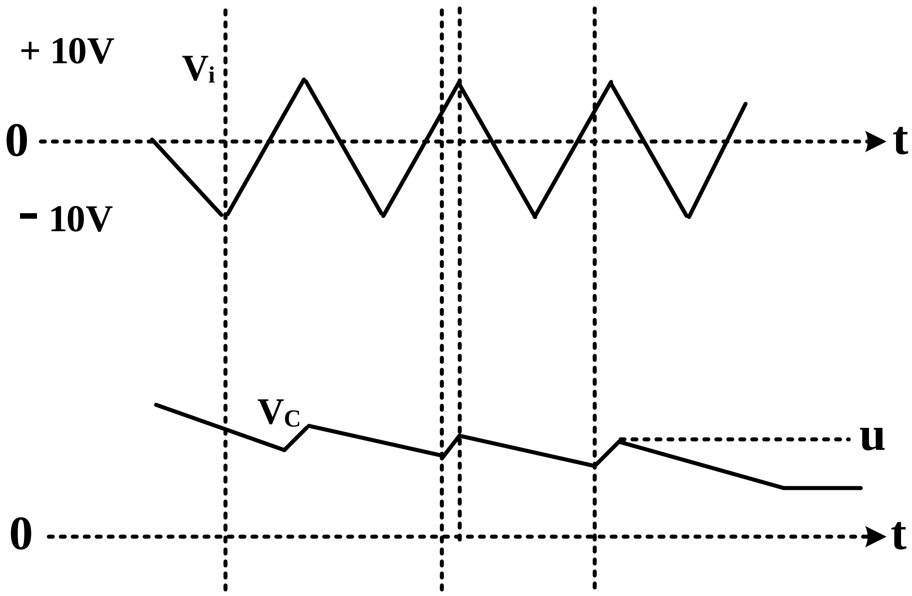

**During positive cycle of input $D_1$ and $D_2$ are shorted thus $V_0 = 0V$**

**During negative cycle the diodes are reverse biased**

$$V_0 = 0V$$

**Thus $V_0 = 0V$ all the times**

15. The figure shows a half-wave rectifier with a 475 µF filter capacitor. The load a draws a constant current $I_0 = 1$ A from the rectifier. The figure also shows the input voltage $V_i$ the output voltage $V_c$ and the peak-to-peak voltage ripple u on $V_c$. The input voltage $V_i$ is a triangle-wave with an amplitude of 10V and a period of 1 ms.




The value of the ripple u (in volts) is ______.

**[GATE 2016: 2 Marks]**

**Soln. Given,**

**Half wave rectifier circuit**

**Filter capacitor = 475 μF**

**Load draws constant current of 1 Amp.**

**The input voltage is triangular.**

**Output voltage $V_c$ is given**

**One has to determine ripple (peak to peak)**

**Amount of charge lost by the capacitor should be equal to the charge gained during charging i.e**

$$I_{de} \,.\, T = V_{r(p-p)} \,.\, C$$

$$\textit{Thus,} \qquad V_{r\,(p-p)} = \frac{I_{dc} \,.\, T}{C} = \frac{1A \,.\times 1 \times 10^{-3}}{475 \times 10^{-6}}$$

$$= \frac{1}{475} \times 10^{3} = 2.1V$$